VME - AIO16

16 Analog Inputs and
4 Analog Outputs
with 16 (12) Bit Resolution

Hardware Manual

PCB version described	AIO16-2

Changes in the chapters

The changed in the manual listed below affect changes in the **hardware** as well as changes in the **description** of facts only.

Chapter	Changes compared to previous version
-	First English edition.

Technical details are subject to change without further notice.

N O T E

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1.1 Block-Circuit Diagram

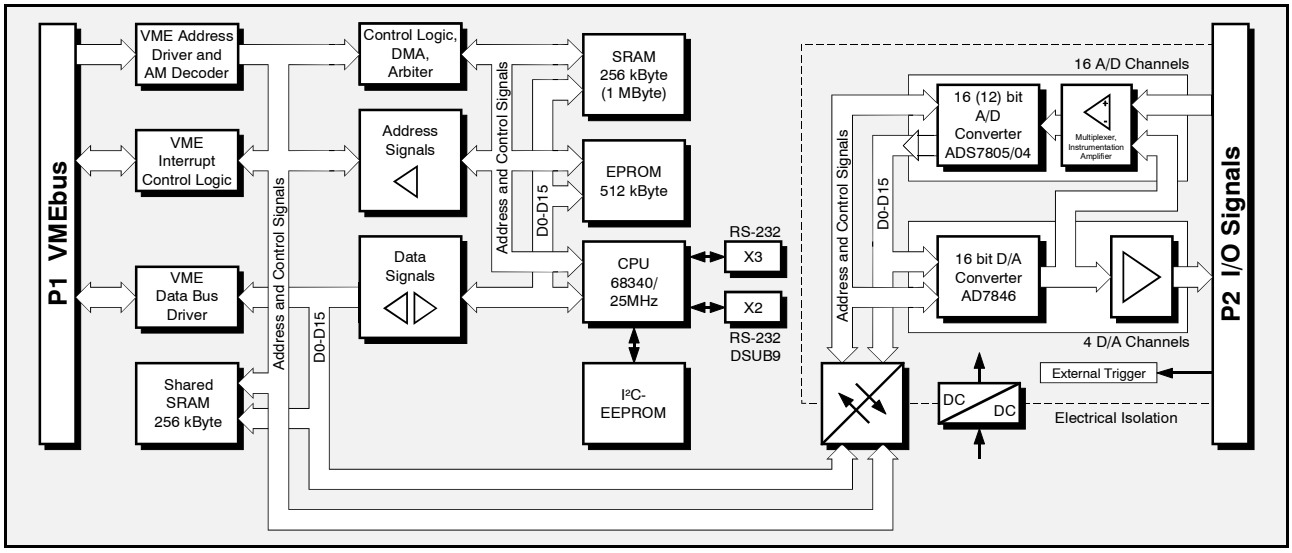


Fig. 1.1.1: Block-circuit diagram of VME-AIO16

The VME-AIO16 is an intelligent VMEbus board which is available with either 6 or 16 analog differential inputs. It can be ideally used for fast flexible signal recording.

The board has got a local CPU 68340 with a clock frequency of 25 MHz to process complex data-recording algorithms. The CPU-unit of the VME-AIO16 has got 256 kbyte SRAM, EPROM and two RS-232-interfaces. Configuration parameters can be stored in an I²C-EEPROM. Additionally the VME-AIO16 has got a 256 kbyte Shared-SRAM, which acts as an interface between local CPU and VMEbus.

The VME-AIO16 has been designed for converters with 16-bit resolution, but it is also available with 12-bit resolution. The input voltage area is ±10 V. By means of using different resistors various other voltages and currents can be achieved (± 20 mA).

The A/D-converters can be synchronized via an external trigger signal. It is of course also possible to trigger via software.

By means of the software included in the package the following sampling rates can be achieved: The maximum sampling rate from trigger signal to the reception of A/D-data in the SRAM is 33 kHz when all 16 channels are synchronously sampled. If the synchronous sampling is restricted to 8 channels the maximum sampling rate is 40 kHz and 45 kHz for one channel.

In addition to the analog inputs the VME-AIO16 has got four bipolar ±10-V-D/A-converter outputs with a resolution of 16 bits. These D/A-converters can be internally used to calibrate and set the offset of the input amplifier. One A/D-converter channel each can be switched to four A/D-inputs for this. The D/A-converter outputs can, of course, also be directly used as process outputs.

All inputs and outputs are completely electrically isolated, making the VME-AIO16 with its rear P2-wiring, its own voltage supply via DC/DC-converters and the LEDs in the front panel ideal for industrial use.

1.2 Summary of Technical Data

1.2.1 General Technical Data

VMEbus interface	IEEE 1014 / C.1
Data-transfer mode	SD16 - slave with A24/D16-access, jumper for pseudo-D32-accesses
Temperature range	max. permissible ambient temperature: 0...50 ˚C
Humidity	max. 90%, non-condensing
Connectors	P1 - DIN 41612-C96 (VMEbus) P2 - DIN 41612-C64 (process I/Os) P3 - socket strip 1 x 32 (A/D-add-on) P4 - socket strip 2 x 25 (A/D-add-on) P5 - socket strip 2 x 20 (optional for DSP-add-on) P6 - socket strip 2 x 20 (optional for DSP-add-on) X1 - 10-pin post connector (BDM-interface) X2 - DSUB9/female (1. serial interface in front panel) X3 - 10-pin post connector (2. serial interface) X4 - pin-contact strip 1 x 6 (optional for DSP-add-on)
Dimensions	160 mm x 233 mm
Slot dimensions	6 HE high / 4 TE wide
Weight	ca. 750 g
Component design	SMD
Power supply	VMEbus P1: 5 V ±5% / 1.0 A VMEbus P1: +12V ±5% -12V ±5% power supply of analog units (±15 VDC, +5 VDC) are generated by DC/DC-converters from +12 V (VME) power supply of optocouplers (+5 VDC) is generated by DC/DC-converters from +5 V (VME)

1.2.2 Micro Processor Units

CPU	16 / 32 bit - µcontroller 68340 / 25 MHz
SRAM	for local CPU: 256 kbyte (optional 1 Mbyte)
Shared SRAM	Shared RAM as communication interface: access possible via VMEbus, local CPU and DSP, capacity: 256 kbyte
EPROM	512 kbyte, organization: 256k x 16, access speed ≤ 120 ns
Watchdog	integrated in CPU 68340
Interrupts	interrupts on VMEbus, level can be programmed, interrupt handler for mailbox interrupts from VMEbus
Serial interfaces	2 serial interfaces RS-232C, maximum 38.4 kbit/s
DSP	optionally available as add-on, type 5600x (The DSP-add-on is not being supported at the moment (09/02)
I²C-EEPROM	for the storage of configuration data

1.2.3 Analog Inputs

Resolution options	16 bit	12 bit
A/D-converters used	ADS7805U	ADS7804U
Linearity (integral)	≤ +2 LSB ($+\Delta U_{MAX} \leq 610\ \mu V$) ≤ -1 LSB ($-\Delta U_{MAX} \leq 305\ \mu V$)	≤ ± 0.45 LSB ($\Delta U_{MAX} \leq 2.2$ mV)
Offset error Gain error (are corrected by local firmware)	≤ 10 LSB ≤ 10 LSB	Bipolar Zero Error: ±10 mV Full Scale Error: ±0.5 %
Digital noise	≤ ±4 LSB	no details
Number of channels	maximum 16, from which 6 equipped on basic board and 10 on add-ons	
Input measuring area	±10 V, option: Different amplifying factors available by equipping different resistors option: Shunt 500 Ω/0.1% to measure current	
Connection	differential	
Sampling rate	programmable up to max. 33 kHz when using all 16 channels, that means 16 new data words every 30µs, sampling rate of 16 channels at automatic offset- and gain-error correction: 10 kHz (8 channels: 15 kHz)	
Trigger	internal or external trigger signal (+5 V) to start conversion	
Voltage sustaining capability	inputs can sustain voltage up to ± 35 V against GND	
Calibration/ multiplexer	multiplexer to connect external analog input signals (P2), signals of the analog output channels, GND or the reference voltage to the A/D-converters	
Electrical insulation	the input units are electrically isolated from the VMEbus potential by means of DC/DC-converters and optocouplers, reference voltage against VMEbus potential in accordance with VDE 0110b §8, insulation group C: 300 VDC / 250 VAC	

1.2.4 Analog Outputs

Number of channels	4
D/A-converters	AD7846
Output voltage range	±10 V
Apparent ohmic resistance	$R_L \geq 600\ \Omega$
Connection	shared reference potential of the four outputs
Resolution	16 bit
Linearity and precision	≤ ± 2 LSB $\Delta U \leq 610\ \mu V$
Electrical insulation	the output units are electrically isolated from the VMEbus potential by means of DC/DC-converters and optocouplers, reference voltage against VMEbus potential in accordance with VDE 0110b §8, insulation group C: 300 VDC / 250 VAC

1.2.5 Real Time Software

In addition to a Shared-RAM interface the local CPU offers the possibility to configure sampling rate, trigger condition etc. This is achieved via the VMEbus.

By means of the multi channelled Shared-RAM interface the VMEbus can also easily be implemented into various master operating system such as OS-9, UNIX, PDOS, VxWorks, VRTX32 or RTOS-UH. C-drivers are available on request.

Please refer to the software manual of the module for more details about the software.

1.3 Order Information

Type	Properties	Order No.
VME-AIO16-16	CPU 68340 / 25 MHz, 256 kbyte SRAM, 16 A/D-channels (16 bit resolution) input voltage range U_{IN} = ±10 V 4 D/A-channels (16 bit resolution)	V.1705.02
VME-AIO16-12	as VME-AIO16, but 16 A/D-channels with 12 bit resolution each	V.1705.04
VME-AIO6-16	as VME-AIO16, but only 6 A/D-channels with 16 bit resolution each	V.1705.03
VME-AIO16-6-12	as VME-AIO16, but only 6 A/D-channels with 12 bit resolution each	V.1705.05
VME-AIO16-RAM1M	with 1Mbyte SRAM instead of 256 kbyte SRAM	V.1705.10
VME-AIO16-OS9	C-driver for OS-9 as source code	P.1705.50
VME-AIO16-VxW	C-driver for VxWorks as source code	P.1705.56
AIO16-ME	English user's manual	M.1705.21

2. PCB-View and Configuration Jumpers

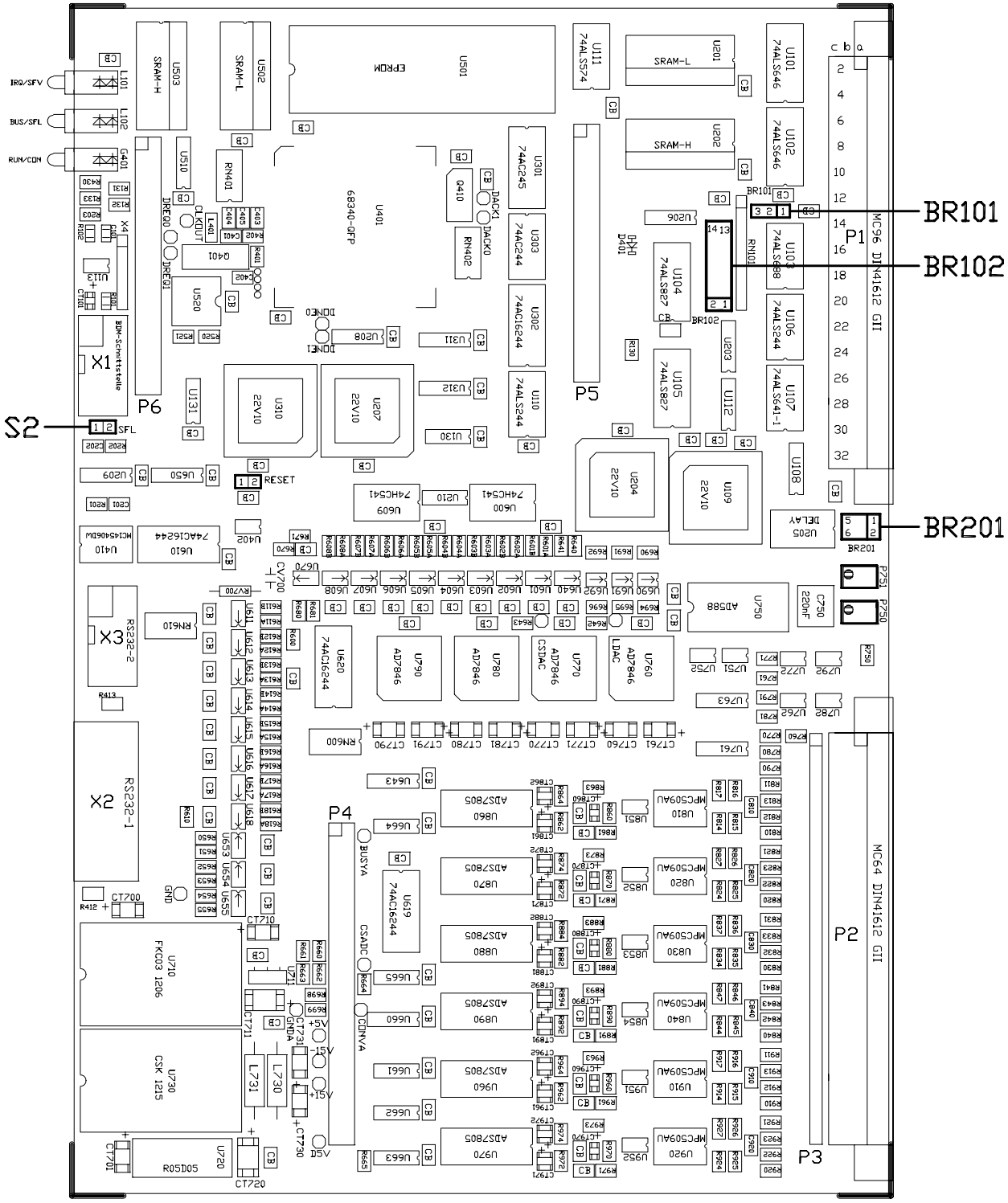


Fig. 2.1.1: Position of jumpers on VME-AIO16

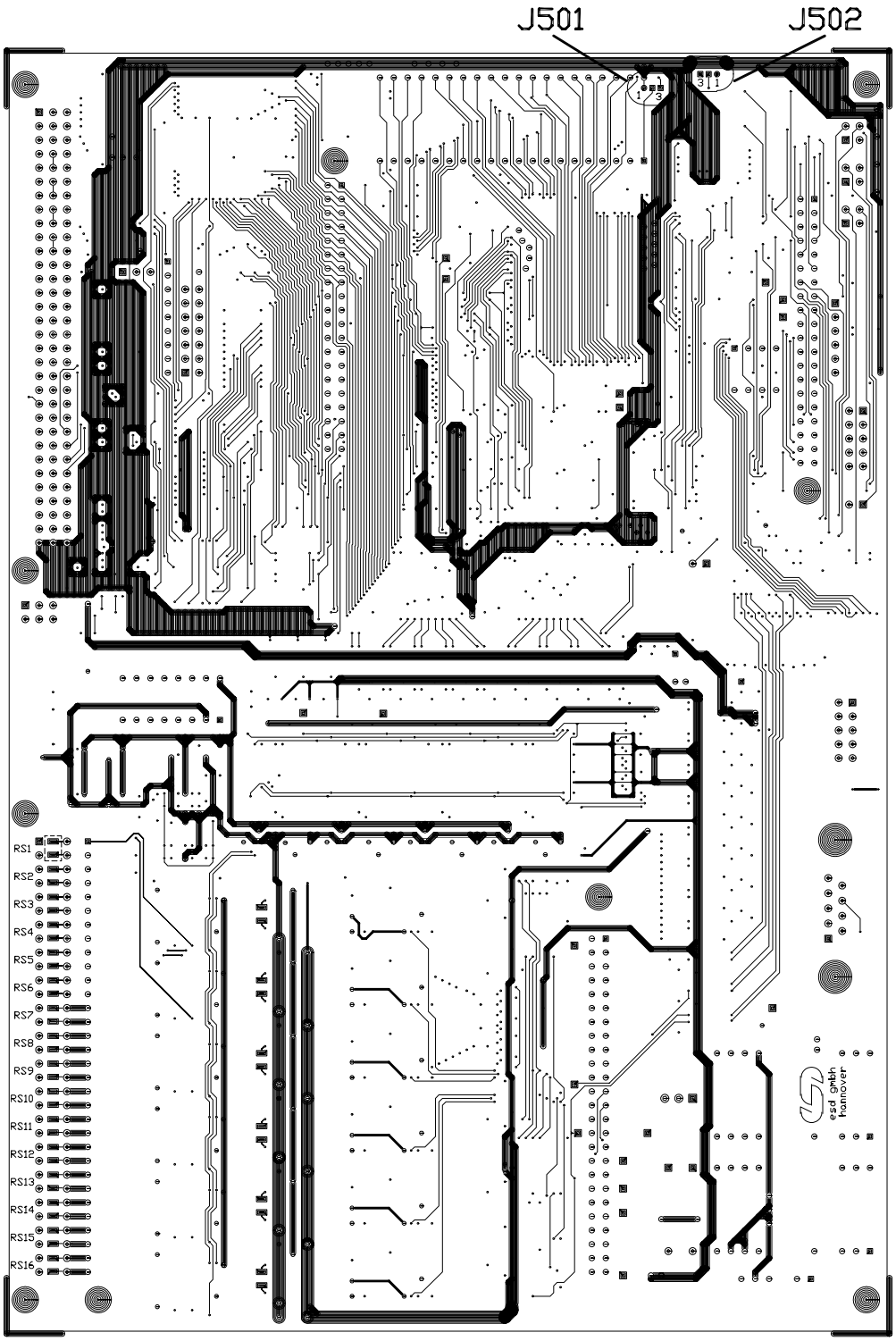
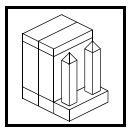


Fig. 2.1.2: Position of solder bridges on bottom layer of PCB



2.1 Default Settings of Bridges

The respective default setting at delivery of the board is shown in the table below.

Please refer to figure 2.1.1 for the position of jumpers. The jumpers will be described below as seen by the user on the PCB with the VMEbus connectors pointing to the right.

Please refer to figure 2.1.2 for the position of the solder bridges. These will be described below as seen by the user on the bottom layer of the PCB with the VMEbus connectors pointing to the left.

Jumper	Function	Setting
BR101	evaluation of VMEbus signal 'LWORD*' (special function: 'D32-don't care')	only accesses with LWORD* = '1' are permitted (D8, D16)
BR102	addresses A19...A23 and AM4 and AM5	VME-base address: $xx68.0000, all A24-standard accessed permitted
BR201	transient response of local control signals (position of jumper must not be changed by user)	DELY3 is assigned wit T3 of the delay line
S2	SYSFAIL at VMEbus	open, that means local SYSFAIL is not passed on to VMEbus

Solder bridge	Function	Setting
J501	memory capacity of EPROM	EPROMs up to 512 kbyte can be used
J502 (*)	memory capacity of SRAM-components	2 SRAMs à 128 kbyte available

(*) SRAM-components are in SMD-design. They are equipped by the manufacturer and cannot be changed by user.

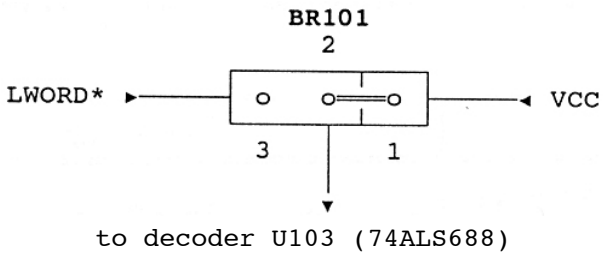
Table 2.1.1: Default setting of bridges at delivery of board

2.2 Evaluation of VMEbus Signal 'LWORD*' (BR101)

By means of this jumper you can select whether the VMEbus signal 'LWORD*' is to be evaluated or whether the level of the signal is to be ignored.

If LWORD* is evaluated, the board only permits D8 or D16-accesses.

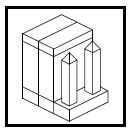
If LWORD* is ignored, ‘pseudo D32-accesses’ to the board are also possible. Only the data lines D0 to D15 are of significance in this mode, however. The VME-AIO16 neither receives nor transmits data on D16 to D31.



Position of jumper BR101	Evaluation of LWORD*	Permissible data accesses
1-2 (VCC at decoder)	no evaluation	D8, D16, D32 (*)
2-3 (LWORD* at decoder)	only accesses with LWORD = '1' are permitted	D8, D16

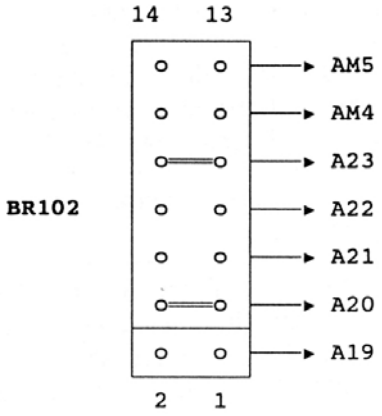
(*) The board permits D32-accesses. Data is only transmitted on D0 to D15, however, because row b of the VMEbus connector P2 of the VME-AIO16 has not been assigned!

Table 2.2.1: Selection for evaluation of VMEbus signal 'LWORD*' via BR101



2.3 Determining the Basis Address and the Address Modifiers via BR102

Jumper open: signal decoded as 'HIGH'
Jumper set: signal decoded as 'LOW'

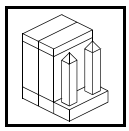


Example:
Default setting at delivery of the board -
basis address $xx68.0000, AM4 = 1, AM5 = 1 ('standard' accesses)

The VME-AIO16 does not evaluate the address modifiers AM0...AM3. The following VMEbus access modes can be configured by means of jumpers:

Address Modifier			permissible VMEbus access modes
AM5	AM4	AM3...AM0	
(0)	(0)	don't care	The ‘extended’-access modes (A23) are available, but these accesses are not being supported by the VME-AIO16! $0E - Extended Supervisory Program Access $0D - Extended Supervisory Data Access $0A - Extended Non-Privileged Program Access $09 - Extended Non-Privileged Data Access
0	1		User-definable access modes (A24) are permissible
(1)	(0)		Short access modes (A16) can be selected, but these accesses are not being supported by the VME-AIO16! $2D - Short Supervisory Access $29 - Short Non-Privileged Access
1	**1**		All ‘standard’ access modes (A24), such as: $3E - Standard Supervisory Program Access $3D - Standard Supervisory Data Access $3A - Standard Non-Privileged Program Access $39 - Standard Non-Privileged Data Access are possible.

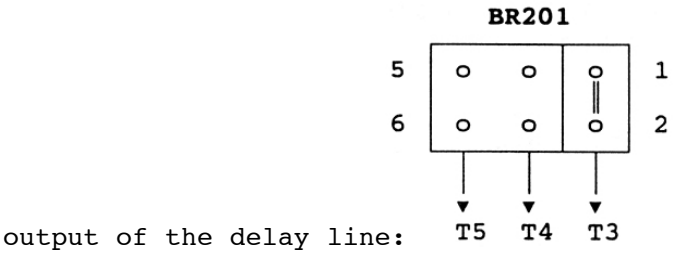
Table 2.3.1: Selecting VMEbus accesses via address modifiers



2.4 Dynamic Response of Local Control Signals (BR201)

By means of this jumper the timing of the local chip-select signals of the memories and the analog units can be changed.

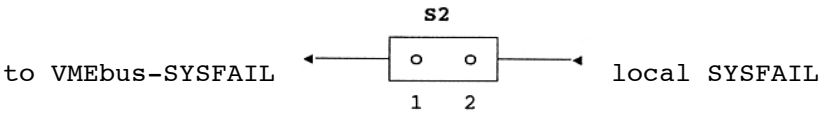
The jumper position must not be changed by the user!



Standard configuration: output T3 of delay line selected

2.5 Enabling the SYSFAIL-Output for the VMEbus (S2)

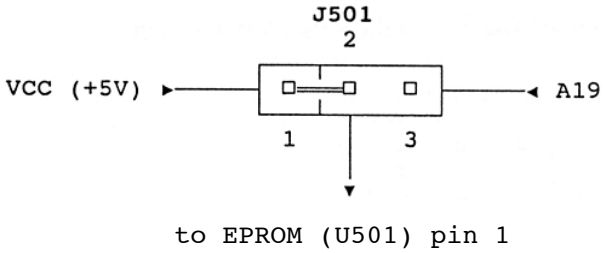
The local SYSFAIL-signal is switched to the VMEbus via S2. The local and the VMEbus-SYSFAIL signal are shown via individual LEDs in the front panel.



Standard configuration: Jumper open, i.e. no SYSFAIL at VMEbus

2.6 Memory Capacity of the EPROM (J501)

Via this solder bridge pin 1 of the EPROM is assigned either with VCC (+5 V) or with address signal A19.

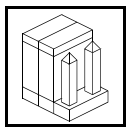


Example: Standard configuration with VCC at pin 1, i.e. EPROMs of up to 512 kbyte can be used.

Solder bridge position J501	Permissible memory capacity of EPROM	Examples for EPROM designs
1-2 (VCC at pin 1)	128 kbyte (1 MBit) 256 kbyte (2 MBit) 512 kbyte (4 MBit)	27C210-120 ns 27C220-120 ns 27C240-120 ns
2-3 (A19 at pin 1)	1 Mbyte (8 MBit)	(*)

(*) EPROMs in centre pinning cannot be used, because they are not pin-compatible.

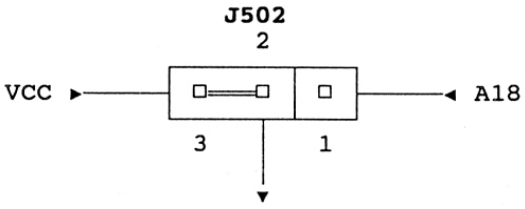
Table 2.6.1: Setting the EPROM-memory capacity via solder bridge J301



2.7 Memory Capacity of SRAM-Components (J502)

By means of this solder bridge pin 30 of the SRAMs is assigned either with VCC (+5 V) or with the local address signal A18.

The SRAM-components are designed in SMD-technology. They are equipped by the manufacturer and cannot be changed by the user. Therefore the position of the solder bridge must not be changed by the user!



Standard configuration: SRAM-component with a capacity of 128 k x 8 bytes are used.

Position of solder bridge J502	Memory capacity of SRAM-components	Examples for SRAM-designs
2-3 (VCC at pin 30)	2 components à (128 k x 8 bytes) = 256 kbyte	*TOSHIBA* TC55100-85
1-2 (A18 at pin 30)	2 components à (512 k x 8 bytes) = 1 Mbyte	*SAMSUNG* KM684000L-L

Table 2.7.1: Setting the SRAM-memory capacity by means of solder bridge J502

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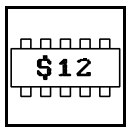


3. Address Assignment of the VME-AIO16

3.1 Address Assignment of Local CPU

The basis addresses of the individual address ranges of the local CPU can be re-programmed. The following table represents the assignment of address ranges for the current firmware initialization:

Address [HEX]	Unit
FFFF.FFFF : FFFF.F000	internal registers of the CPU 68340 (see manual 68340)
FFFF.EFFF : FFFF.E000	local I/Os in least significant data word (mailbox-interrupt handling, local control signals)
00C3.FFFF : 00C0.0000	EPROM
0083.FFFF : 0080.0000	Shared area (A/D-converter, D/A-converter, mailbox interrupts)
0003.FFFF : 0000.0000	SRAM of CPU 68340

Table 3.1.1: Address ranges of the local CPU

$FFFF.E000 + Address offset [HEX]	Unit/registers
3E : 30	Write Acknowledge (acknowledge for VMEbus-IRQ, A/D-IRQ, D/A-IRQ and Trigger VMEbus-Interrupt)
2E : 20	Write Latch (VMEbus-Interrupt-Level, Convert-Multiplexer...)
1E...10	not assigned
0E : 00	DSP-communication (is not being supported)

Table 3.1.2: Assignment of the local I/O-area (access only via local CPU 68340)

3.2 Shared-Address Range (Addresses of Local CPU and VMEbus)

The shared-address range acts as an interface between the local CPU and the VMEbus. The VMEbus master and the local CPU can access these cells.

The following table shows the relative addresses of the local CPU in the first column and the addresses relative to the VMEbus-base address of the VME-AIO16 in the second column:

Access via local CPU `$0080.0000+` address offset [HEX]	Access via VMEbus: VMEbus base + address offset [HEX]	Component/signal	
		Write access	Read access
3FFFE	7FFFC	not assigned	read out A/D-converter 16-value
3FFFC	7FFF8	not assigned	read out A/D-converter 15-value
3FFFA	7FFF4	not assigned	read out A/D-converter 14-value
3FFF8	7FFF0	not assigned	read out A/D-converter 13-value
3FFF6	7FFEC	WRIVEC (Write VMEbus-IRQ-Vector)	read out A/D-converter 12-value
3FFF4	7FFE8	SWCOM (local IRQ via VMEbus -> activates commander)	read out A/D-converter 11-value
3FFF2	7FFE4	activate DACDMAREQ	read out A/D-converter 10-value
3FFF0	7FFE0	SWCONV (start A/D-conversion)	read out A/D-converter 9-value
3FFEE	7FFDC	activate SWLDAC	read out A/D-converter 8-value
3FFEC	7FFD8	activate SWLDAC	read out A/D-converter 7-value
3FFEA	7FFD4	activate SWLDAC	read out A/D-converter 6-value
3FFE8	7FFD0	activate SWLDAC	read out A/D-converter 5-value
3FFE6	7FFCC	activate SWLDAC	read out A/D-converter 4-value
3FFE4	7FFC8	activate SWLDAC	read out A/D-converter 3-value
3FFE2	7FFC4	activate SWLDAC	read out A/D-converter 2-value
3FFE0	7FFC0	activate SWLDAC	read out A/D-converter 1-value

Access via local CPU $0080.0000 + address offset [HEX]	Access via VMEbus: VMEbus base + address offset [HEX]	Component/signal	
		Write access	Read access
3FFD6	7FFAC	set D/A-converter 4 with SWLDAC	read out D/A-converter 4-value from RAM-cell 4.4
3FFD4	7FFA8	set D/A-converter 3 with SWLDAC	read out D/A-converter 3-value from RAM-cell 3.4
3FFD2	7FFA4	set D/A-converter 2 with SWLDAC	read out D/A-converter 2-value from RAM-cell 2.4
3FFD0	7FFA0	set D/A-converter 1 with SWLDAC	read out D/A-converter 1-value from RAM-cell 1.4
3FFC6	7FF8C	set D/A-converter 4 without SWLDAC	read out D/A-converter 4-value from RAM-cell 4.1
3FFC4	7FF88	set D/A-converter 3 without SWLDAC	read out D/A-converter 3-value from RAM-cell 3.1
3FFC2	7FF84	set D/A-converter 2 without SWLDAC	read out D/A-converter 2-value from RAM-cell 2.1
3FFC0	7FF80	set D/A-converter 1 without SWLDAC	read out D/A-converter 1-value from RAM-cell 1.1
3FFBE : 00000	7FF7C : 00000	256 Kbyte Shared SRAM less the AD/DA-converter range, 16-bit data width, on VMEbus accessible via every second WORD-address	

Table 3.2.1: Assignment of shared-areas with addresses of the VMEbus and the local CPU

3.3 Notes on the Shared-Address Range

A write access to the D/A-converters simultaneously assigns cells of the shared-RAM with D/A-values. A read access then leads to the SRAM and the previously set value can be played back.

Attention: Setting a D/A-value without SWLDAC (**S**oft**w**are **L**atch **D**/**A**-**C**onverter) as well as setting a D/A-value with SWLDAC trigger write accesses to different RAM-cells! The D/A-value must therefore always be played back via the same address used when setting the D/A-value, otherwise the wrong value might be played back!

The signal SWLDAC, which is connected in parallel to all D/A-converters, initiates the conversion. Write accesses without SWLDAC only load the new value into the D/A-converter. Only when setting SWLDAC the new value will be converted.

Note : Write-accessing via SWLDAC therefore sets the new D/A-value of the converter selected and simultaneously starts the conversion of all D/A-channels!

4. Description of Units

4.1 Interrupt Handling

Interrupt levels and vectors are completely managed by the local firmware and must not be changed by the user!

4.1.1 Assignment of Interrupt Inputs of CPU 68340

The CPU 68303 has got four external interrupt inputs which have been assigned on the VME-AIO16 as shown below:

68340-interrupt input	Assignment	Note
IRQ3	IRQCOM* (local interrupt triggered by VMEbus)	Auto Vector (address $6C)
IRQ5	IRQDAC* (D/A-converter)	Auto Vector (address $74)
IRQ6	IRQADC* (A/D-converter)	Auto Vector (address $78)
IRQ7	not assigned	-

Table 4.1.1: 68340-interrupt input connections

4.1.2 VMEbus-Slave-Interrupt Logic

The VMEbus-slave-interrupt logic offers the possibility to trigger an interrupt on the VMEbus via the VME-AIO16. In addition a local interrupt (SWCOM*) can be generated on the VME-AIO16.

4.1.2.1 Generating a VMEbus-Interrupt

The interrupt level of the VMEbus interrupt can be programmed via an addressable 1-bit latch and a decoder.
The interrupt level is selected via the inputs of the decoder:

Decoder-input signals with according relative address			VMEbus-interrupt level
VLEV3 $24	VLEV2 $22	VLEV1 $20	
0	0	0	no interrupt
0	0	1	IRQ1
0	1	0	IRQ2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

Table 4.1.2: Setting the VMEbus-interrupt level via decoder inputs

Signals VLEV1, VLEV2 and VLEV3 are configured via an addressable latch. By means of the data bit D15 the level of these signals is determined (D15 = '1' -▸ VLEVx = '1').

Via address bits A1 to A3 the according signals is selected. The relative addresses are shown in the table above. As basis you have to specify the address of the local I/O-area ($FFFF.E000 -> current default value -> this I/O-base address can be re-programmed via the registers of the local CPU, it is therefore subject to change.)

In order to program the interrupt level the decoder input signals have to be configured in accordance with the table above. This can be achieved by write-accessing the address of the desired bit (VLEV1...VLEV3). Data bit D15 has to have the desired level of the bit. Data bits D0 to D14 will not be evaluated. Following a RESET all bits will be ‘0’.

In addition the VMEbus interrupt has to be enabled via the local signal VINTEN*. This signal is set directly by port PB0 of CPU68340. The interrupt will be enabled, if the signal is set to ‘0’.

The interrupt is triggered via the local signal VIRQ*, which is activated with D15 = '0' via the relative address $2E (basis address: $FFFF.E000, subject to change).
Receiving the VMEbus-interrupt acknowledge cancels the interrupt again.

4.1.2.2 Programming the VMEbus-Interrupt Vector

The vector which is put out to the VMEbus during the interrupt-acknowledge cycle can be programmed on the shared-area address $3FFF6 (basis address $0080.0000, subject to change).

4.1.2.3 Generating a Local Interrupt via VMEbus (SWCOM*)

Via the VMEbus an interrupt (SWCOM: **S**oft**w**are **Com**munication) of the local CPU can be triggered. This is achieved via a WORD-write access to address $7FFE8 (relative to the basis address of the VME-AIO16). The data transmitted during the access will not be evaluated and can therefore be set arbitrarily.

The interrupt is directly triggered via input IRQ3 of the CPU 68340. It generates an auto-vector.

The interrupt is managed by the local firmware. Please refer to the software manual for a detailed description of interrupt handling.

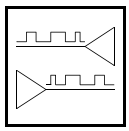
RESET

4.2 Voltage Monitoring and RESET

When the voltage falls below the operating-voltage tolerance (U < 4.65 V) and during power-up a RESET of local CPU 68340 will be triggered.

The local CPU is also reset via the VMEbus-RESET signal. For test matters a local RESET can be triggered via jumper S401.

The RESET resets all local units and the local software!



4.3 Serial Interfaces

4.3.1 Configuration

Both RS-232-interfaces of the VME-AIO16 are controlled by the CPU 68340. The interfaces have been designed for a bit rate of 1,200 to 38400 bit/s.

The first serial interface can operate in XON/XOFF- as well as modem operation. The second interface can only be operated without hardware handshake.

The interfaces have been specified as represented below:

	1. serial interface	2. serial interface
Bit rate	19,200 baud	9,600 baud
Data bits	8	8
Stop bits	1	1
Parity	no Parity	no Parity
Handshake	XON/XOFF	XON/XOFF

Table 4.3.1: Default setting of serial interfaces

	Value range
bit rate [b-aud]	38,400 ; 19,200 ; 9,600 ; 4,800 ; 2,400 ; 1,200
Data bits	5, 6, 7, 8
Stop bits	1, 2
Parity	none, odd, even
Handshake	XON/XOFF (no options at the moment)

Table 4.3.2: Possible configurations of the serial interfaces (not yet implemented)

4.3.2 Connecting the Serial Interfaces

Below the wiring of both RS-232-interfaces is represented. The figures explain the signal abbreviations used in the appendix (Connector Assignment).

The connector assignment of the RS-232-interfaces and the signal term is specified exemplary for the connection if the VME-AIO16 as receiver (modem, DCE).
The assignment of the 9-pin DSUB-connectors of the second RS-232-interface results as represented, if the DSUB-terminal is connected to the 10-pin post connector X3 via a flat-ribbon cable (1:1).

4.3.2.1 First RS-232-Interface (Port 1)

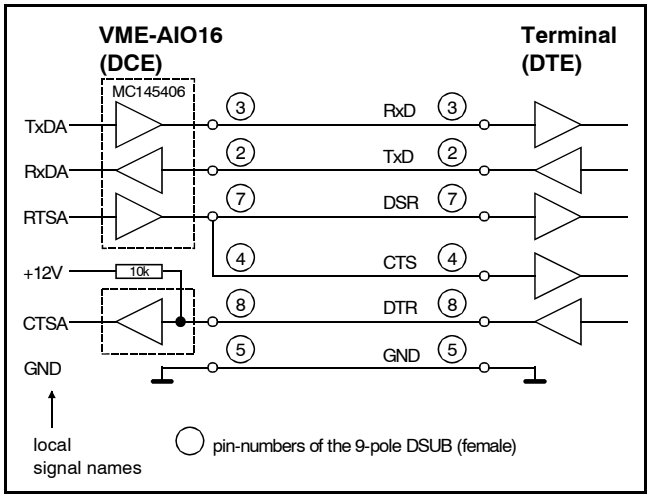


Fig. 4.3.1: Connection of first RS-232-interface

4.3.2.2 Second RS-232-Interface (Port 2)

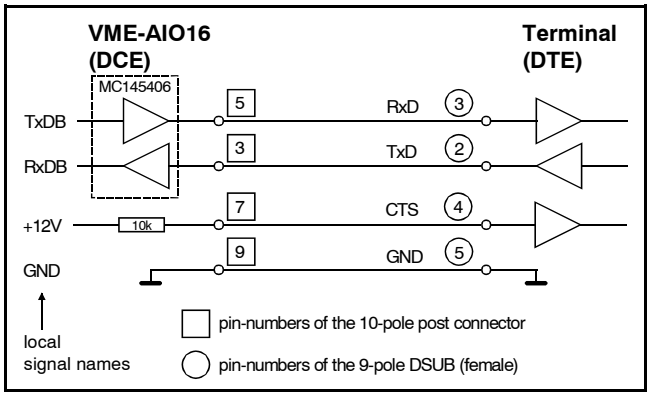
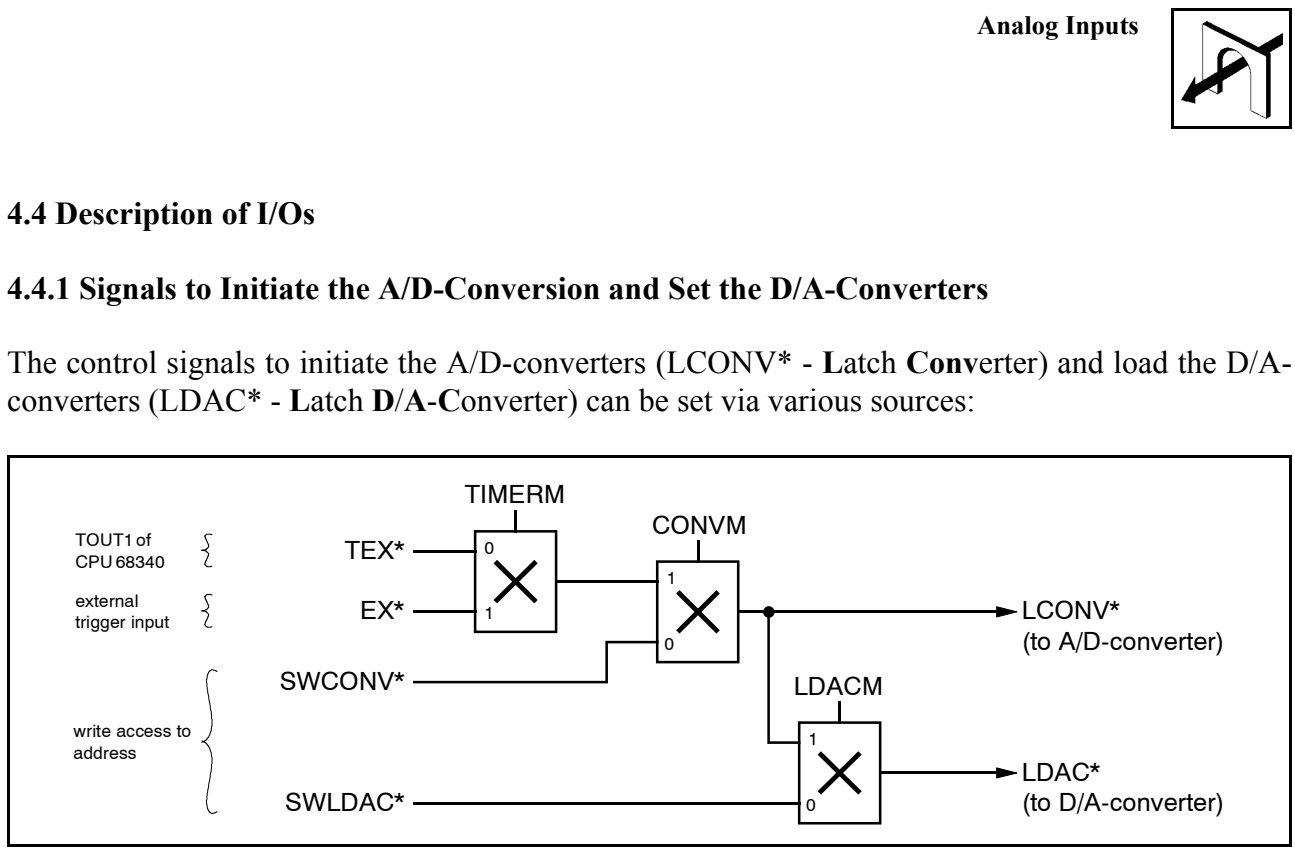


Fig. 4.3.2: Connection of second RS-232-interface



4.4 Description of I/Os

4.4.1 Signals to Initiate the A/D-Conversion and Set the D/A-Converters

The control signals to initiate the A/D-converters (LCONV* - **L**atch **Conv**erter) and load the D/A-converters (LDAC* - **L**atch **D**/**A**-**C**onverter) can be set via various sources:

Fig. 4.4.1: Overview of multiplexer circuit of control signals of the converters

The upper branch of the schematic circuit diagram represents the activation of the A/D-converter. The signal LCONV* is generated in default setting of the multiplexers (all multiplexers set to '0') via software by means of control signal SWCONV* (**S**oft**w**are **Conv**ert). SWCONV* is set via a read access to the relative addresses $3FFEE (local CPU) or $7FFE0 (VMEbus) as described in chapter 'Shared-Address Range'.

Via the multiplexer signal CONVM (**Conv**ert **M**ultiplexer) either the timer output of the CPU 68340 (TOUT1) or the external trigger signal (EX*) can be used to initiate the conversion instead of the software converter.

Please refer to the manual of the CPU 68340 for programming the CPU-timer. The external trigger signal will be described in the following chapter ‘Trigger Input’.

The multiplexer signal TIMERM is generated via CPU-port pins OP4 and OP6.

OP6	OP4	Multiplexer circuit (TIMERM)
0	0	not useful
0	1	timer output
1	0	external trigger
1	1	neither timer nor trigger

Table 4.4.1: Setting the multiplexer TIMERM via CPU-ports

The multiplexer signal CONVM is set via the local relative address $26 in the I/O-range (basis address: $FFFF.E000 (subject to change)). A write access with data bit D15= '1' also sets signal CONVM to '1'. Bits D0 to D14 are not being evaluated.

The D/A-converter puts out a new value via signal LDAC. SWLDAC can be set when loading a new D/A-value or be activated separately. The address which are accessible via these signals have been described in the previous chapter 'Shared-Address Range'.

By switching via the multiplexer signal LDACM the convert signal of the A/D-converters can be used to set the D/A-converters instead of using the SWLDAC-signals. When setting up a control device this has got the advantage that the newly calculated D/A-value is always put out exactly after a sample period of the A/D-converter.

Signal LDACM is set via the local relative address $2A in the I/O-range (basis address: $FFFF.E000 (subject to change)). Write-accessing via data bit D15 = '1' sets signal LDACM also to '1'. Bits D0 to D14 are not being evaluated.

The multiplexer circuit can be parameterized completely by means of the local firmware. Therefore it is not necessary for the user to change the multiplexer bits individually via write accesses!

4.4.2 Analog Inputs

Six of the 16 analog inputs of the VME-AIO16 have been equipped on the basic board and 10 on an add-on. The inputs are electrically isolated along with the analog outputs via DC/DC-converters and optocouplers.

All 16 input channels have been structured identically: Depending on the resolution desired an ADS7805 or an ADS7804 is used as A/D-converter per channel. Further essential components are the input multiplexer MPC509A and the instrument amplifier INA118. The figure below represents the input circuit of the first channel.

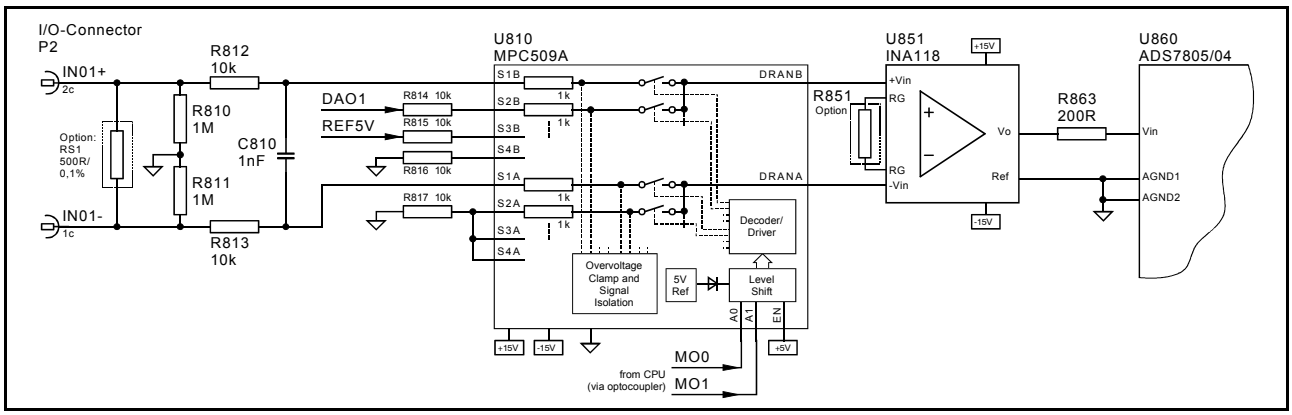


Fig 4.4.1: Circuit of analog inputs (example: channel 1)

Via the multiplexers MPC509A the inputs can be assigned with GND, +5 V-reference voltage or the output signals of the D/A-converters for adjustment. Each A/D-channel has got a separate multiplexer. The 16 multiplexers are driven in parallel that means that all converter inputs are always assigned to GND, for instance, simultaneously.

Via the local signals MO0 and MO1, which are again set via CPU-ports PA0 and PA1, the multiplexers are driven. Like all other control signals these are also isolated from the CPU-units by means of optocouplers.

The following table represents the assignment of analog inputs in dependence from the levels of the CPU-ports:

Control bits of multiplexers		Assignment of A/D-converter inputs
CPU-port PA1 (MO1*)	CPU-port PA0 (MO0*)	
0	0	external input signal of P2
0	1	D/A-converter output
1	0	reference voltage +5 V
1	1	analog reference potential GND

Table 4.4.1: Controlling the multiplexers via CPU-ports

Since only four D/A-converter channels are available, these are assigned to the A/D-inputs as follows:

D/A-converter channel	Adjustment of A/D-channel
1	1, 5, 9, 13,
2	2, 6, 10, 14,
3	3, 7, 11, 15,
4	4, 8, 12, 16,

Table 4.4.2: Assignment of D/A-converters to A/D-channels at adjustment

In the analog input circuit the amplifying factor of the instrument amplifier INA118 can be changed for each channel via the optionally equippable resistor RG. If the resistor has not been equipped, the amplification is '1' and the analog inputs have been designed for a voltage swing of max. ± 10 V. The amplification (V) can be increased via RG as follows:

$$V = 1 + \frac{50\ k\Omega}{RG}$$

In order to be able to measure currents in the range of ± 20 mA resistors RS1 to RS16 are optionally equippable. These SHUNTs with 500 Ω/0.1% are equipped on the bottom layer of the PCB between the pins of I/O-connector P2.

The reference voltage of the A/D-converters is generated by a highly precise reference device (AD588) which has been fine-tuned via a potentiometer by the manufacturer.

The A/D-conversion can be initiated via software (SWCONV) or an external trigger signal (please also refer to the following chapter).

The conversion period of an A/D-converter is about 8 µs. In order to determine the actual sampling rate the delays caused by reprocessing have to be taken into account. The manner of data processing is determined via software. The software therefore has an essential influence on the sampling rates that can be achieved.

Among other features the VME-AIO16 offers the chance to read back data via DMA-cycles and store it in the SRAM. Furthermore the offset and gain errors of the analog inputs can be corrected by the local firmware.

4.4.3 Trigger Input

The VME-AIO16 has got a trigger input via which the conversion of all A/D-channels can be initiated simultaneously. The input is activated when a voltage of + 5 V is applied.

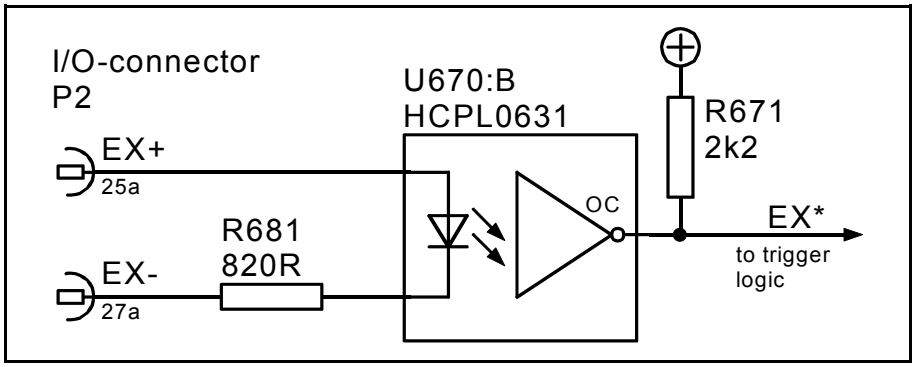
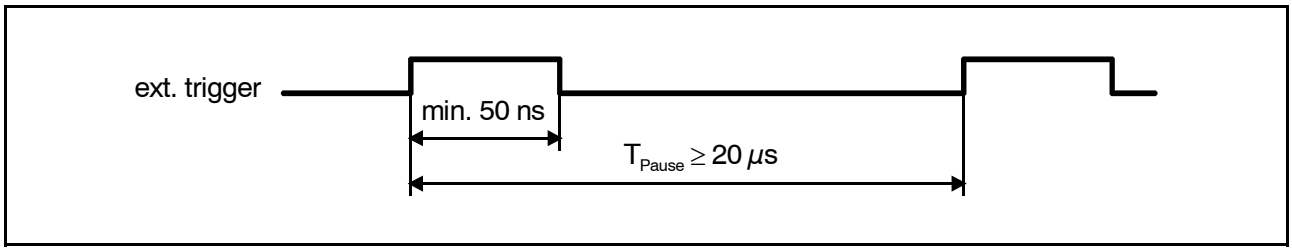
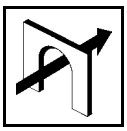


Fig. 4.4.2: Input circuit of trigger signal

On load side of the input circuit a monoflop has been connected which extends the input pulse to the length required.

For the pulse width of the external trigger signal the following limit values have to be adhered to (evaluation of 16 channels, local DMA-operation):





4.4.4 Analog Outputs

The four analog outputs of the VME-AIO16 have been structured identically. An AD7846 with 16 bit resolution is used as D/A-converter. The maximum voltage swing of the outputs has been determined at ± 10 V.

Between the D/A-converter and the output amplifier OPA27 an ADG211/212 has been connected as multiplexer. By means of this multiplexer the analog output can be assigned with GND or the D/A-converter output signal via CPU-port PA2. This offers the advantage that the outputs can be switched off following a RESET, but the D/A-converter inputs can also be used to adjust the analog inputs without applying the D/A-signals to I/O-connector P2 during adjustment.

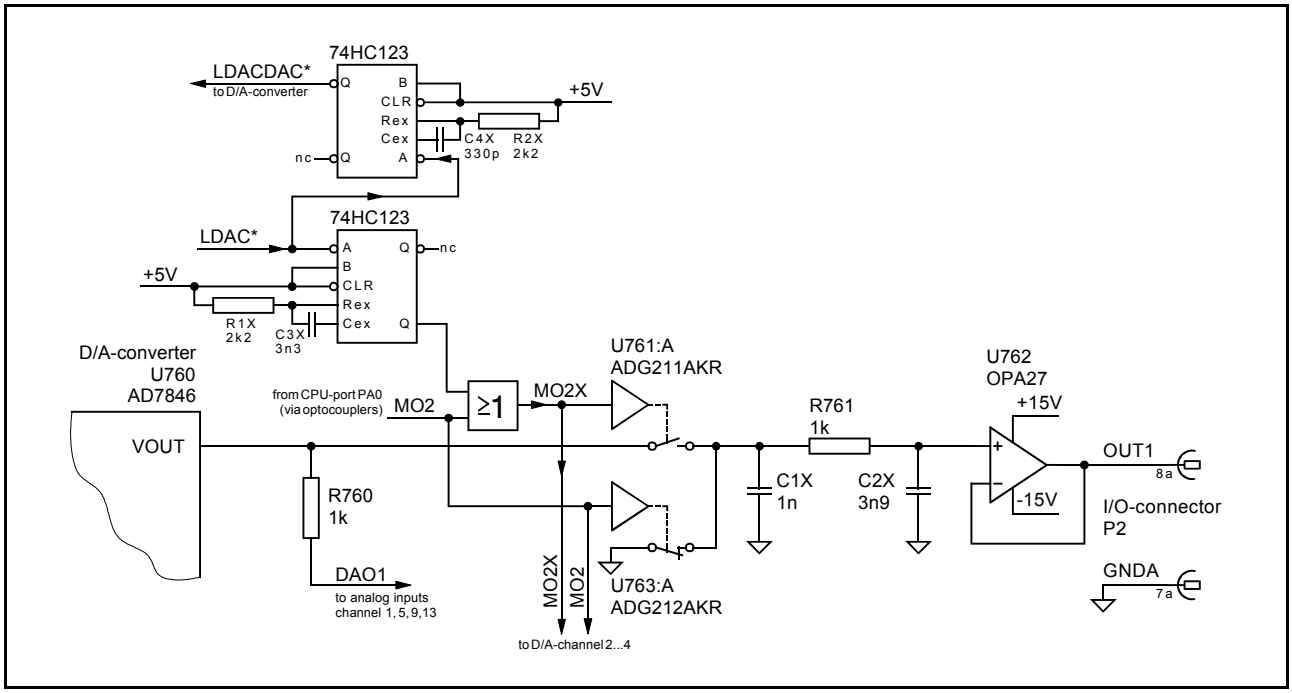


Fig. 4.4.3: Circuit of analog outputs (example: channel 1)

The multiplexer is also used in connection with monoflop 74HC123 as 'sample & hold' to improve the transient response of the D/A-output:

The D/A-converter AD7846 causes a voltage peak of about 30 mV at its output at falling and rising edge of the LDAC-signal (**L**atch **D**/**A**-**C**onverter). By means of the multiplexer the D/A-converter is isolated from the output operation amplifier during these voltage variations. Capacitor C1X retains the last voltage value of the D/A-converter during this period. After the conversion the DAC is reconnected again. The minimal voltage peaks occurring during this are eliminated by the RC-block R761-C2X connected on load side.

The following time chart represents the relations between the individual signals:

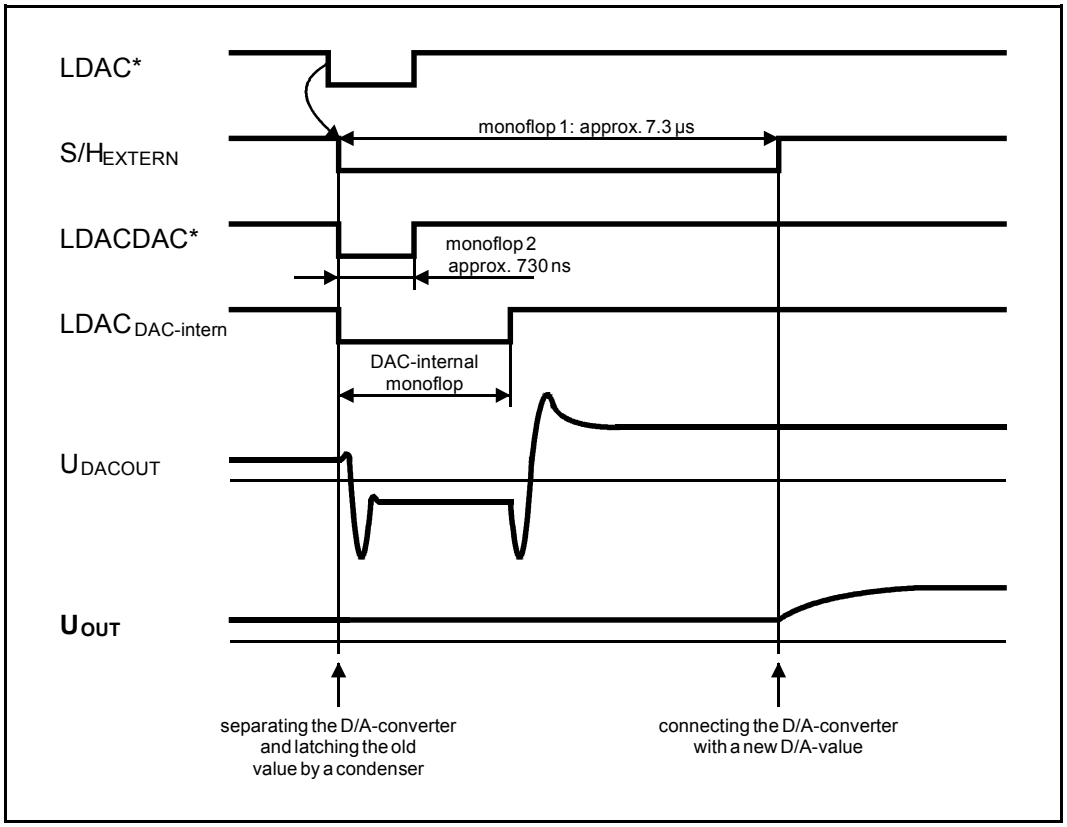
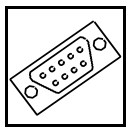


Fig. 4.4.4: Avoiding voltage peaks at analog outputs via an external sample & hold-circuit

The outputs are electrically isolated along the analog inputs via DC/DC-converters and optocouplers.

The reference voltages of the A/D-converters are generated by a highly precise voltage reference device (AD588, not shown here) which has been fine-tuned via a potentiometer by the manufacturer.



5. Appendix

5.1 Connector Assignments

5.1.1 VMEbus P1

Pin	Row a	Row b	Row c
1	D00	-	D08
2	D01	-	D09
3	D02	-	D10
4	D02	BG0IN* ⌉	D11
5	D04	BG0OUT* ⌋	D12
6	D05	BG1IN* ⌉	D13
7	D06	BG1OUT* ⌋	D14
8	D07	BG2IN* ⌉	D15
9	GND	BG2OUT* ⌋	GND
10	-	BG3IN* ⌉	SYSFAIL*
11	GND	BG3OUT* ⌋	-
12	DS1*	-	SYSRESET*
13	DS0*	-	LWORD*
14	WRITE*	-	AM5
15	GND	-	A23
16	DTACK*	-	A22
17	GND	-	A21
18	AS*	-	A20
19	GND	-	A19
20	IACK*	GND	A18
21	IACKIN*	-	A17
22	IACKOUT*	-	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12 V	-	+12 V
32	+5 V	+5 V	+5 V

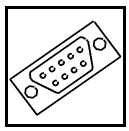
Multipoint connector in accordance with DIN41612 design C96/a+b+c
I_{max} per pin : 1.0 A

⌉⌋ ... signals bridged on PCB
- ... signal not connected on PCB

5.1.2 I/O-Connector P2

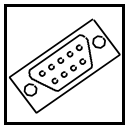
Assignment of a 64-pin transient module					
Pin	Assignment of I/O-connector P2				Pin
	Row a	Signal		Row c	
2	1	GNDA	IN01-	1	1
4	2	OUT4	IN01+	2	3
6	3	GNDA	IN02-	3	5
8	4	OUT3	IN02+	4	7
10	5	GNDA	IN03-	5	9
12	6	OUT2	IN03+	6	11
14	7	GNDA	IN04-	7	13
16	8	OUT1	IN04+	8	15
18	9	GNDA	IN05-	9	17
20	10	GNDA	IN05+	10	19
22	11	:	IN06-	11	21
24	12	:	IN06+	12	23
26	13	:	IN07-	13	25
28	14	:	IN07+	14	27
30	15	:	IN08-	15	29
32	16	:	IN08+	16	31
34	17	:	IN09-	17	33
36	18	:	IN09+	18	35
38	19	:	IN10-	19	37
40	20	:	IN10+	20	39
42	21	:	IN11-	21	41
44	22	:	IN11+	22	43
46	23	:	IN12-	23	45
48	24	GNDA	IN12+	24	47
50	25	EX+	IN13-	25	49
52	26	-	IN13+	26	51
54	27	EX-	IN14-	27	53
56	28	-	IN14+	28	55
58	29	-	IN15-	29	57
60	30	-	IN15+	30	59
62	31	-	IN16-	31	61
64	32	-	IN16+	32	63

I/O-connector: Clip connector DIN41612 design C64/a+c
I_{max} per pin : 1.0 A
- ... signal not connected
Turn to the following page for signal description.



5.1.3 Description of Signals of P2

INx-, INx+	differential analog inputs (max. ± 10 V) (x = 1, 2, ...16)
OUTx	analog outputs (± 10 V) (x = 1, 2, 3, 4)
GNDA	reference potential of analog units
EX+, EX-	external trigger input to synchronously start the A/D-converters (0V - OFF, +5V - ON)



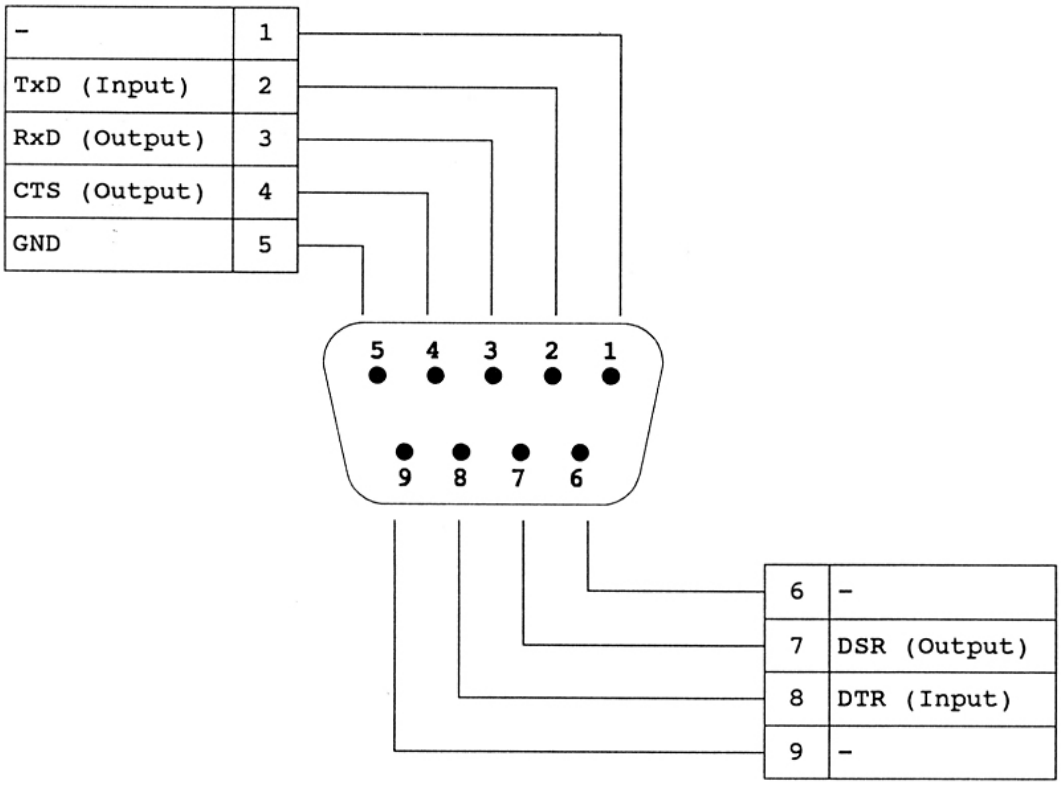
5.1.4 Serial Interfaces Port 1 and Port 2

The two serial interfaces comply with RS-232C. The bit rate has been preset to 19200 bit for port 1 and 9600 bit for port 2 and can be reprogrammed.

Port 1 is connected to a 9-pin female DSUB in the front panel (X2). Port 2 is only assigned with RxD and TxD and accessible via a 10-pin socket strip (X3).

Below the signal terms will be stated as seen from the terminal (transmitter, DEE). The direction of the signals given in brackets is as seen from the VME-AIO16.

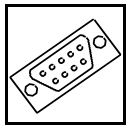
5.1.4.1 Assignment of the 9-Pin Female DSUB X2



- ... signal not connected

The signal designated as DTR at the DSUB-connector is locally connected to input signal ‘CTSA’ and also with a 10 kΩ Pull-Up-resistor at +12 V.

The signals designated as CTS and DSR at the DSUB-connector are controlled on board by the local signal ‘RTSA’.



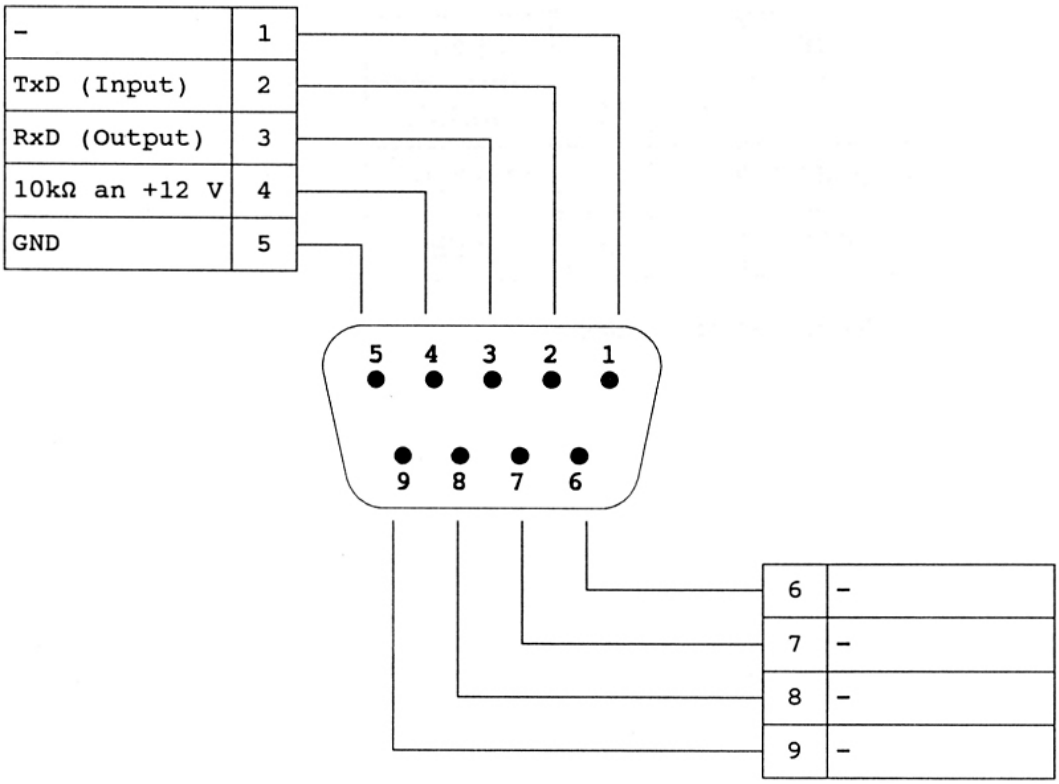
5.1.4.2 Assignment of 10-Pin Post Strip X3

Signal	Pin		Signal
-	1	2	-
TxD (input)	3	4	-
RxD (output)	5	6	-
via 10 kΩ at +12 V (CTS)	7	8	-
GND	9	10	-

10-pin post connector

- ... signal not connected

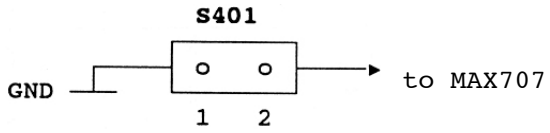
If X4 is connected to a 9-pin female DSUB 1:1 via a flat-ribbon cable, the following assignment results:



- ... signal not connected

5.1.5 RESET-Key Switch Connection (S401)

The local RESET signal of the VME-AIO16 can be activated via post connector S401 for test matters.

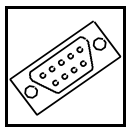


The RESET is triggered, if the pins of the post strip are connected.

5.1.6 BDM-Interface (X1)

Signal	Pin		Signal
DS*	1	2	BERR*
GND	3	4	BKPT*
GND	5	6	FREEZE
RESET*	7	8	IFETCH*
VCC	9	10	IPIPE*

10-pin post connector



5.1.7 Connectors for A/D-Converter Add-On (P3, P4)

P3

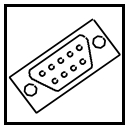
Pin	Signal
1	DA01
2	DA01
3	DA02
4	DA02
5	DA03
6	DA03
7	DA04
8	DA04
9	REF25
10	REF25
11	REF5
12	REF5
13	IN07-
14	IN07+
15	IN08-
16	IN08+
17	IN09-
18	IN09+
19	IN10-
20	IN10+
21	IN11-
22	IN11+
23	IN12-
24	IN12+
25	IN13-
26	IN13+
27	IN14-
28	IN14+
29	IN15-
30	IN15+
31	IN16-
32	IN16+

socket strip 1x32

P4

Signal	Pin		Signal
MO0	1	2	MO1
AD0	3	4	AD1
AD2	5	6	AD3
AD4	7	8	AD5
AD6	9	10	AD7
AD8	11	12	AD9
AD10	13	14	AD11
AD12	15	16	AD13
AD14	17	18	AD15
AA1	19	20	AA2
AA3	21	22	AA4
CONV*	23	24	CONVD*
CS07*	25	26	CS08*
CSADC*	27	28	BUSYP1
BUSYP2	29	30	-
-	31	32	-
+5 V	33	34	+5 V
+5 V	35	36	+5 V
-15 V	37	38	-15 V
+15V	39	40	+15 V
GNDA	41	42	GNDA
GNDA	43	44	GNDA
GNDA	45	46	GNDA
GNDA	47	48	GNDA
GNDA	49	50	GNDA

socket strip 2x25



5.1.8 Connectors for Optional DSP-Add-On (P5, P6, X4)

P5

Signal	Pin		Signal
LD0	1	2	LD1
LD2	3	4	LD3
LD4	5	6	LD5
LD6	7	8	LD7
LD8	9	10	LD9
LD10	11	12	LD11
LD12	13	14	LD13
LD14	15	16	LD15
LA1	17	18	LA2
LA3	19	20	LA4
LA5	21	22	LA6
LA7	23	24	LA8
LA9	25	26	LA10
LA11	27	28	LA12
LA13	29	30	LA14
LA15	31	32	LA16
LA17	33	34	LREAD*
LDS0*	35	36	LDS1*
LAS*	37	38	LDTACK*
DSPREQ*	39	40	DSPACK*

socket strip 2x20

P6

Signal	Pin		Signal
D8	1	2	D9
D10	3	4	D11
D12	5	6	D13
D14	7	8	D15
A1	9	10	A2
A3	11	12	CSDSP*
R/W*	13	14	RESET*
SWCONV*	15	16	SWADREQ*
SWCOM*	17	18	DREQ0*
DREQ1*	19	20	DB1
DB2	21	22	DB3
DB4	23	24	DB5
VCC	25	26	VCC
VCC	27	28	VCC
VCC	29	30	VCC
VCC	31	32	VCC
GND	33	34	GND
GND	35	36	GND
GND	37	38	GND
GND	39	40	GND

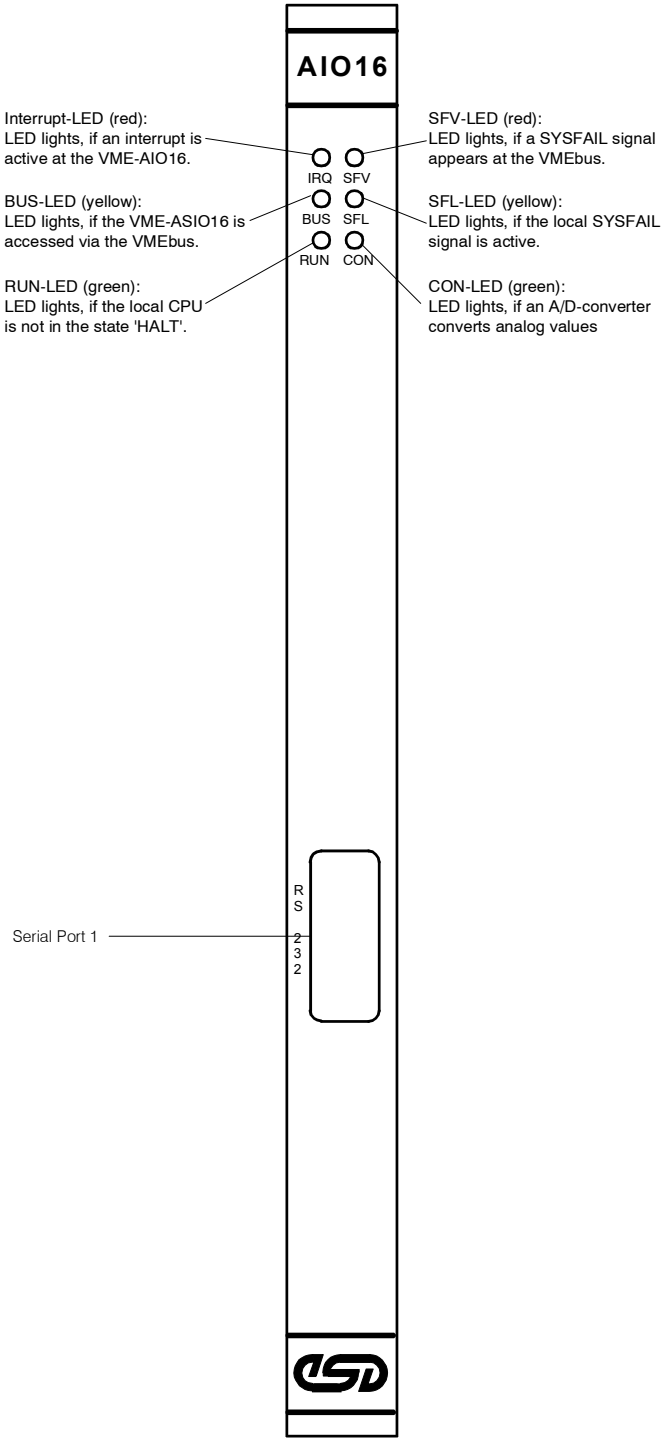
socket strip 2x20

X4

Pin	Signal
1	DB1
2	DB2
3	DB3
4	DB4
5	DB5
6	DB6

post strip 1x6

5.2 Front Panel



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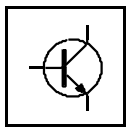

5.3 Circuit Diagrams

The PDF-file of this document does not contain the circuit diagrams. The circuit diagrams are shipped on request.

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