

PMC-FIFO

2 * 16-bit FIFO (4k, 16k or Compatible)

8-bit TTL Input with IRQ

8-bit TTL Input Static

8-bit TTL Output

Hardware Manual

NOTE

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Document file:	I:\TEXTE\DOKU\MANUALS\SONSTIGE\PMC_FIFO\PMFIF6HE.MA6
Date of print:	1.12.99

PCB version:	PMCFIFO-10
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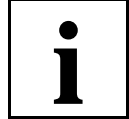
Changes in the chapters

The changes in the user's manual listed below affect changes in the hardware as well as changes in the description of the facts only.

Chapter	Changes versus previous version
1.2,3	designation of the I/O-Connector P1 corrected
-	

Technical details are subject to change without notice.

Content	Page
1. Overview	3
1.1 Module Description	3
1.2 General Technical Data	4
1.3 Technical Data of the I/O-Circuits	5
1.4 Order Information	6
2. FIFO Memory	7
3. Appendix	9
3.1 Connector Pin Assignments	9
3.1.1 Assignment of the 64-pole PMC-Connector P11	9
3.1.2 Assignment of the 64-pole PMC-Connector P12	10
3.1.3 Assignment of the 68-pole I/O-Connector P1	11



1. Overview

1.1 Module Description

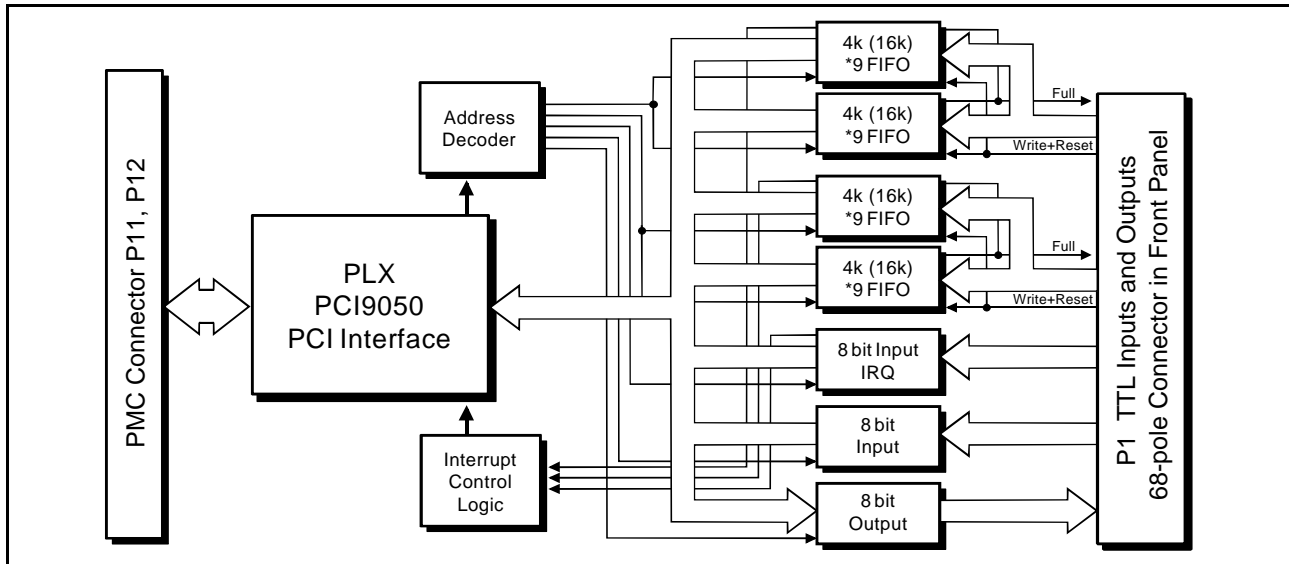


Fig. 1.1.1: Block diagram of PMC-FIFO

The module PMC-FIFO is supported with 2x 16 FIFO inputs for TTL level signals. The FIFOs can be equipped as 4k-size, 16k-size or compatible circuits. Reading-in the FIFO inputs is controlled by two externally available write inputs. By two RESET inputs the FIFOs can be deleted externally. For a flexible read-out the FIFOs can generate interrupts at 'Empty', 'Half-Full', and 'Full'.

Furthermore the module has another 16 inputs and 8 outputs, which can be read or set by TTL-registers or TTL-drivers. 8 of the inputs can trigger an interrupt on the module.

After a power-on or when receiving the RESET signal, all FIFOs and interrupts are deleted and the 8 digital outputs are set to 'high'.

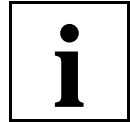
The TTL-inputs and outputs are connected by a 68-pole male contact in the front panel.



1.2 General Technical Data

Module Interface	<i>PMC</i>
Temperature range	0...70EC ambient temperature
Humidity	max. 90%, non-condensing
Connectors	P11 - <i>PMC</i> 64-pole P12 - <i>PMC</i> 64-pole P1 - 68-pole, Typ: Thomas&Betts: 311-068072E (TTL-I/O signals via front panel) with Thomas&Betts: 311-068302 as necessary match
Board dimensions	74 mm x 149 mm
Weight	ca. 100 g
Power supply	via <i>PMC</i> : 5V / ca. 500mA

Table 1.2.1: General data of the *PMC-FIFO*



1.3 Technical Data of the I/O-Circuits

Number of FIFO inputs	2 * 16 (4k or 16k each) 2 * FIFO Write, 2 * FIFO Reset
Timing of the FIFO inputs (refer page 7)	data setup time: t_s \$ 20 ns data hold time: t_H \$ 20 ns data cycle time: t_p \$ 50 ns burst read rate: # 132 Mbyte/s non burst read rate: # 4 Mbyte/s
Number of FIFO outputs	2 * FIFO-Full-Flag
Number of digital inputs with interrupt capability	8
Number of digital inputs	8
Number of digital outputs	8
Voltage level (all I/Os)	TTL-level
Receiver (IRQ-inputs, Write signals of FIFOs and FIFO reset)	74LS14 (Schmitt-trigger with hysteresis)
Receiver (all other inputs)	74LS244
Transmitter (FIFO-Full-Flag)	74LS244
Transmitter (8-bit output)	74ALS573
Interrupts	- FIFO IRQ at 'empty', 'half full' and 'full' - 8 digital inputs with interrupt (edge 'high to low')

Table 1.3.1: Technical data of the I/O circuits



1.4 Order Information

Type	Features	Order No.
PMC-FIFO	PMC-module with 2x 16-bit FIFO, 8-bit input (with IRQ), 8-bit input, 8-bit output	V.2010.01
PMC-FIFO-OS9	Driver as C-source for OS9	V.2010.50
PMC-FIFO-VxWorks	Driver as C-source for VxWorks	V.2010.56
PMC-FIFO-RTOS-UH	Driver for RTOS-UH	V.2010.54
PMC-FIFO-MD (*)	English user's manual	V.2010.20

1*) If ordered together with the module, the manual is free of charge.

Table 1.4.1: Order information

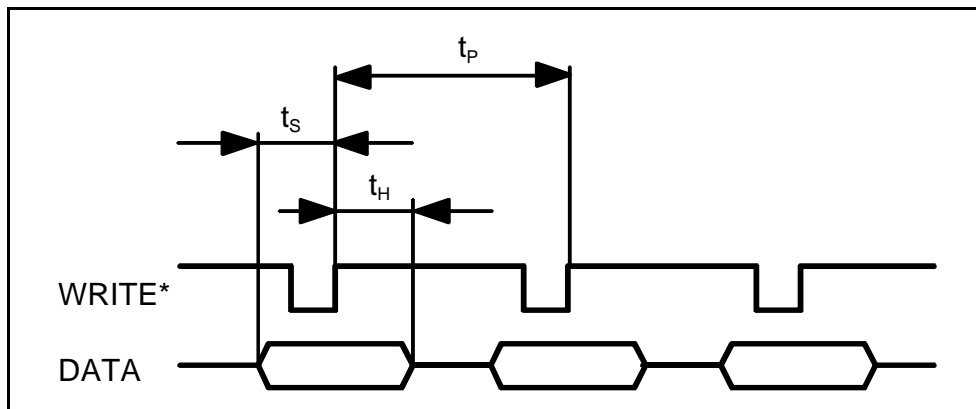


2. FIFO Memory

The used FIFO memory components are of type Cypress CY7C433 (4k depth) or CY7C462 (16k depth) or compatible components.

The following figure displays the FIFO-write timing for reading data. Data is sampled at rising edge of the WRITE signal. Data has to be valid at least 20 ns before the rising edge appears (setup time t_s) and has to be hold at least 20 ns after the rising edge of the WRITE signal (hold time t_H)

The minimum cycle time for reading data is 50 ns (t_p) resulting a write frequency of maximum 20 Mhz.



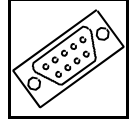
t_s \$ 20 ns

t_H \$ 20 ns

t_p \$ 50 ns

Fig. 2.1: FIFO Write Timing

Reading of the FIFOs is done with a data rate of up to 132 Mbyte/s in burst mode (DMA controller). Without burst mode the maximum data rate is 4 Mbit/s.



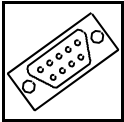
3. Appendix

3.1 Connector Pin Assignments

3.1.1 Assignment of the 64-pole PMC-Connector P11

Pin #	Signal Name	Signal Name	Pin #
1	TCK	-12V	2
3	GND	INTA*	4
5	INTB*	INTC*	6
7	PMCPRSNT*	+5V	8
9	INTD*	-	10
11	GND	-	12
13	CLK	GND	14
15	GND	PMCGNT*	16
17	PMCREQ*	+5V	18
19	+5V	AD31	20
21	AD28	AD27	22
23	AD25	GND	24
25	GND	C/BE3*	26
27	AD22	AD21	28
29	AD19	+5V	30
31	+5V	AD17	32
33	FRAME*	GND	34
35	GND	IRDY*	36
37	DEVSEL*	+5V	38
39	GND	LOCK*	40
41	SDONE*	SBO*	42
43	PAR	GND	44
45	+5V	AD15	46
47	AD12	AD11	48
49	AD09	+5V	50
51	GND	C/BE0*	52
53	AD06	AD05	54
55	AD04	GND	56
57	+5V	AD01	58
59	AD02	AD01	60
61	AD00	+5V	62
63	GND	REQ64*	64

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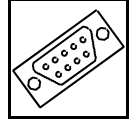
Connector Pin Assignment

3.1.2 Assignment of the 64-pole PMC-Connector P12

Pin #	Signal Name	Signal Name	Pin #
1	+12V	TRST*	2
3	TMS	TDO	4
5	TDI	GND	6
7	GND	-	8
9	-	-	10
11	-	-	12
13	RST*	-	14
15	-	-	16
17	-	GND	18
19	AD30	AD29	20
21	GND	AD26	22
23	AD24	-	24
25	IDSEL	AD23	26
27	-	AD20	28
29	AD18	GND	30
31	AD16	C/BE2*	32
33	GND	-	34
35	TRDY*	-	36
37	GND	STOP*	38
39	PERR*	GND	40
41	-	SERR*	42
43	C/BE1*	GND	44
45	AD14	AD13	46
47	GND	AD10	48
49	AD08	-	50
51	AD07	-	52
53	-	-	54
55	-	GND	56
57	-	-	58
59	GND	-	60
61	ACK64*	-	62
63	GND	-	64

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- This pin is not connected at the board.



3.1.3 Assignment of the 68-pole I/O-Connector P1

Pin #	Signal Name	Signal Name	Pin #
1	F1D0	F2D12	35
2	F1D1	F2D13	36
3	F1D2	F2D14	37
4	F1D3	F2D15	38
5	F1D4	F2WRITE*	39
6	F1D5	F2RESET*	40
7	F1D6	F2FULL*	41
8	F1D7	GND	42
9	GND	IRQ0	43
10	F1D8	IRQ1	44
11	F1D9	IRQ2	45
12	F1D10	IRQ3	46
13	F1D11	IRQ4	47
14	F1D12	IRQ5	48
15	F1D13	IRQ6	49
16	F1D14	IRQ7	50
17	F1D15	GND	51
18	F1WRITE*	IN0	52
19	F1RESET*	IN1	53
20	F1FULL*	IN2	54
21	GND	IN3	55
22	F2D0	IN4	56
23	F2D1	IN5	57
24	F2D2	IN6	58
25	F2D3	IN7	59
26	F2D4	GND	60
27	F2D5	OUT0	61
28	F2D6	OUT1	62
29	F2D7	OUT2	63
30	GND	OUT3	64
31	F2D8	OUT4	65
32	F2D9	OUT5	66
33	F2D10	OUT6	67
34	F2D11	OUT7	68

Type of I/O-Connector on the board (male contact): Thomas&Betts: 311-068072E

Type of necessary mating connector at the line (female contact): Thomas&Betts: 311-068302