

PMC-CPU/405

**PowerPC™ Module
with CAN and ETHERNET**



Hardware Manual

to Product V.2020.xx

Document File:	I:\texte\Doku\MANUALS\PMC\PMC-405\Englisch\PMC-405_13H.en9
Date of print:	11.05.2005

PCB:	PPC-405 from revision 1.1 with serial number from ABxxxx (PPC-405 revision 1.0 up to serial number AAxxxx is described in hardware manual revision 1.1)
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Changes in the chapters

The changes in the document listed below affect changes in the hardware as well as changes in the description of the facts, only.

Chapter	Changes as compared with previous version
1.2.7	Software support updated.
-	-

Technical details are subject to change without further notice.

NOTE

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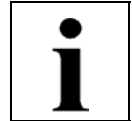
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1. Overview

1.1 Description of the PMC-CPU/405 Board

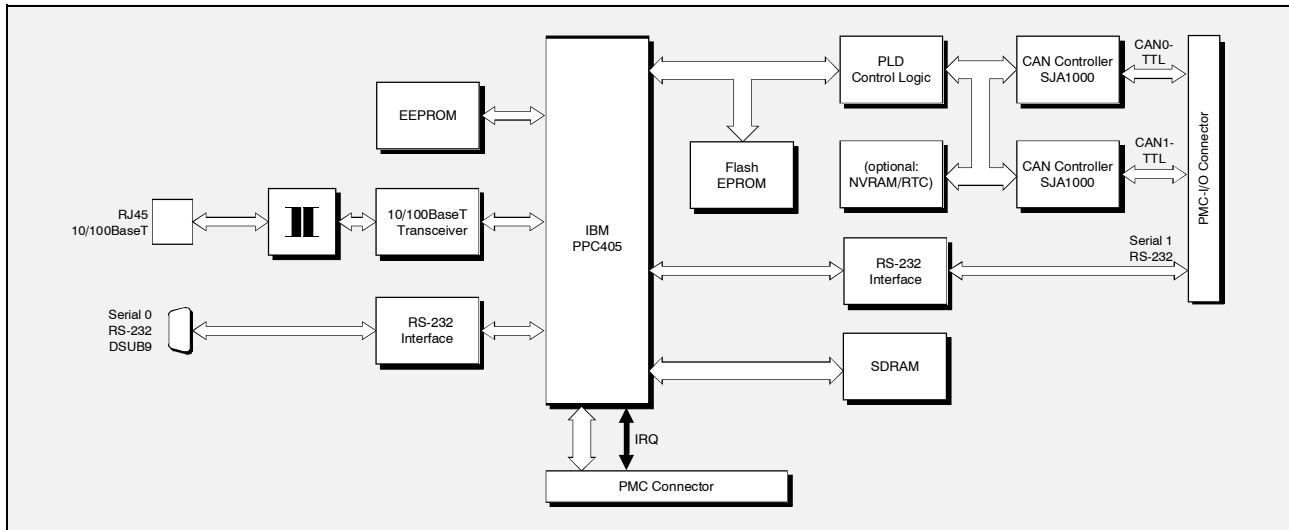


Fig. 1.1.1: Block circuit diagram

The PMC-CPU/405 is a PMC-board in ‘Single’ PCI Mezzanine Card format. It is available as PMC monarch or as non-monarch board.

Apart from a powerful CPU the PowerPC 405GP processor has got an SDRAM controller, a PCI bus interface, a controller for serial interfaces and an MII-interface which is used to realize an ETHERNET interface.

In addition to Flash EPROM and an optional NVRAM as system memory, the PMC-CPU/405 has got up to 128 Mbytes SDRAM as working memory.

Both serial interfaces are designed as RS-232 interfaces. One can be accessed via a DSUB9-connector in the front panel. The second serial interface is accessible via a PMC-I/O connector.

The two CAN interfaces are controlled by SJA1000 CAN controllers and they are suitable for transmission rates up to 1 Mbit/s. The TTL-signals of both controllers are led to the PMC-I/O connector.

The ETHERNET interface is suitable for 10 Mbit and 100 Mbit networks. They are connected via an RJ45-socket in the front panel.

The LEDs in the front panel show the current status of the PMC-CPU/405 module.



1.2 Summary of Technical Data

1.2.1 General Technical Data

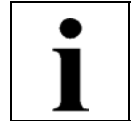
Ambient temperature	0...50 °C
Humidity	max. 90 %, non-condensing
Power supply	via PMC bus, 5 V <u>and</u> 3.3 V
Connectors	P11 (64-pin PMC connector) - PCI signals P12 (64-pin PMC connector) - PCI signals P14 (64-pin PMC connector) - CAN-TTL interfaces CAN0 and CAN1, Serial 1 (RS-232 interface) X700 (9-pin DSUB, male) - Serial 0 (RS-232 interface) X720 (8-pin SMD socket) - Debug interface X1100 (8-pin RJ45 socket) - ETHERNET Twisted Pair (IEEE 802.3)
Dimensions	148.33 mm x 74.04 mm
Weight	100 g

Table 1.2.1: General technical data

1.2.2 PCI Bus

Host bus	PCI bus in accordance with PCI Local Bus Specification 2.2
PCI data	32 bits
Processor	PowerPC™ 405GP
Interrupt	Non-monarch version: Interrupt signal A Monarch version: Interrupt signal A, B, C, D

Table 1.2.2: PCI bus interface



1.2.3 Microprocessor and Memory

CPU	PPC 405GP / 200 MHz (max. 266 MHz) / 32 bit
NVRAM	optional, 32 K x 8 bits (optional: RTC instead of NVRAM)
Flash-EEPROM	up to 4 M x 16 bit (8 Mbyte) Flash EPROM
Serial EEPROM	1 Kbyte
SDRAM	8 M x 32 bit (32 Mbyte) (default) up to 32 M x 32 bit (128 Mbyte) (option)

Table 1.2.3: Microprocessor and memory

1.2.4 Serial Interface

Number	2
Controlled	PPC 405GP
Bit rate	Microcontroller: 300 bit/s ... 115.200 bit/s RS-232 transceiver: max. 115.200 bit/s
Physical interface	Serial 0: RS-232C, Serial 1: RS-232C
Connectors	Serial 0: 9-pin DSUB-connector (male) in the front panel Serial 1: 64-pin PMC-connector on the board

Table 1.2.4: Serial interface

1.2.5 CAN Interfaces

Number	2
CAN controller	SJA1000
CAN protocol	CAN 2.0A/2.0B
Physical interface	TTL-level
Transmission rate	10 Kbit/s ... 1Mbit/s
Bus termination	has to be terminated externally
Connectors	64-pin PMC-I/O connector (Pn4/Jn4 32 bit PCI)

Table 1.2.5: CAN-interfaces



1.2.6 ETHERNET-Interface

Number	1
Bit rate	10 Mbit/s, 100 Mbit/s
Processor	PPC 405GP
Physical interface	Twisted Pair (IEEE802.3) 10/100BaseT
Electrical isolation	via repeating coil
Connector	8-pin RJ45-socket in front panel

Table 1.2.6: ETHERNET-interface

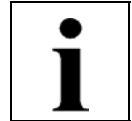
1.2.7 Software Support

The boot monitor *U-Boot* *is stored in the Flash memory. This makes it possible for the PMC-CPU/405 to boot with various operating systems from the network or the local Flash memory.

The operating systems Linux and VxWorks are available with corresponding drivers for the local interfaces. Further operating systems are available on request.

Furthermore the CAN-transmission protocols CANopen and DeviceNet and a local WEB-server are available.

* <http://sourceforge.net/projects/u-boot/>



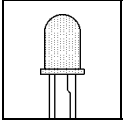
1.2.8 Order Information

Type	Properties	Order No.
PMC-CPU/405	PMC Monarch IBM PPC 405GP, 200 MHz, 32 MB SDRAM, 4 MB Flash	V.2020.02
PMC-CPU/405-64	as V.2020.02 but 64 MB SDRAM	V.2020.03
PMC-CPU/405-A	as V.2020.02 but PMC Non-monarch	V.2020.12
PMC-CPU/405-VxW	VxWorksBSP	V.2020.30
PMC-CPU/405-Linux	Linux BSP/adaption	V.2020.32
PMC-CPU/405-MD	Manual in English 1*) (this manual)	V.2020.21
PMC-CPU/405-ENG	Engineering manual in English 2*) Content: circuit diagrams, PCB top overlay drawing, data sheets of significant components	V.2020.25

1*) The manual is free, if it was ordered together with the product.

2*) The manual is liable for costs, please contact our support

Table 1.2.8: Order information



Front Panel View with LED-Display

2. Front Panel View with LED-Display

The module has got three LEDs in the front panel.

2.1 LEDs in the Front Panel

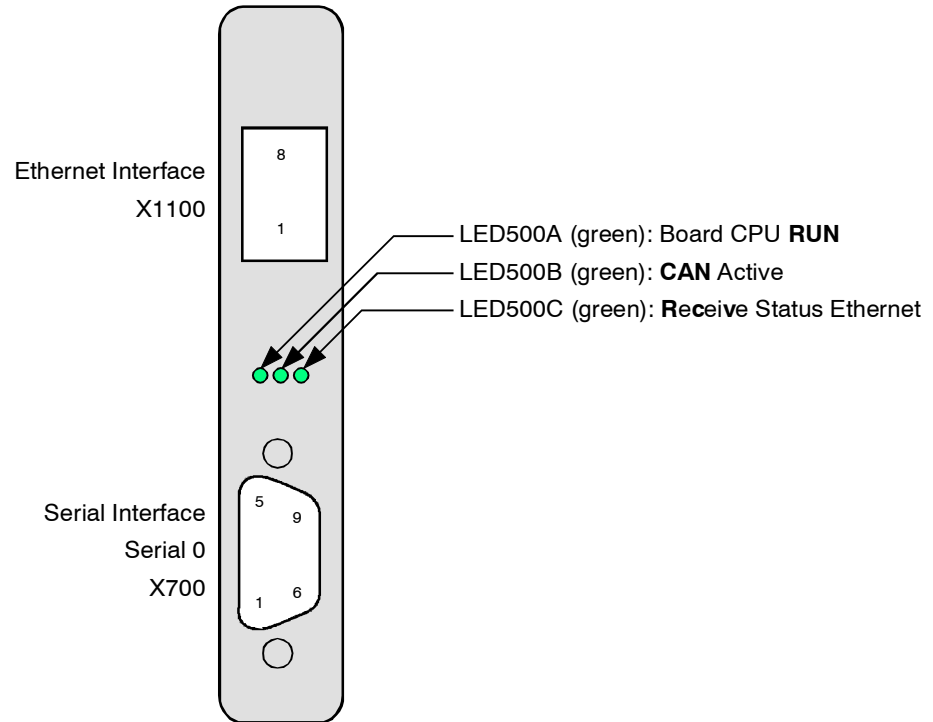
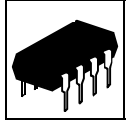


Fig. 2.1.1: Position and colour of the LEDs

LED	Colour	Name	Display function (LED on)
LED500A	green	CPU-ACT-LED	local CPU is in RUN status (LED lights at every access to the SDRAM. The LED can be blinking or constantly on in normal operation)
LED500B	green	CAN-IRQ-LED	CAN-frames are being transmitted or received
LED500C	green	RCV	Receive-Status ETHERNET (reception of ETHERNET-data packages)

Table 2.1.1: Display function of LEDs



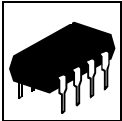
3. Description of the Units

3.1 PowerPC 405GP Microprocessor

3.1.1 General

The general functions of the PowerPC 405GP will not be explained in this manual. The manual of the processor can be downloaded from the homepage of the manufacturer IBM, at:

<http://www-3.ibm.com/chips/products/powerpc>



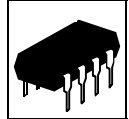
Description of the Units

3.1.2 Address-Assignment

Start address [HEX]	End address [HEX]	Unit
0x0000_0000	0x03FF_FFFF	SDRAM (max. 64 Mbyte)
0x8000_0000	0xEF5F_FFFF	PCI core memory area
		Internal periphery:
0xEF60_0300	0xEF60_0307	UART0-register (see PPC 405GP manual table 3-6 , page 3-9) *
0xEF60_0400	0xEF60_0407	UART1-register (see PPC 405GP manual table 3-7 , page 3-10) *
0xEF60_0500	0xEF60_0510	IIC0-register (see PPC 405GP-manual table 3-8 , page 3-11)
0xEF60_0600	0xEF60_0601	OPB-arbiter register (see PPC 405GP manual table 3-9 , page 3-12)
0xEF60_0700	0xEF60_077F	GPIO-controller register (see PPC 405GP manual table 3-10 , page 3-13)
0xEF60_0800	0xEF60_0867	Ethernet register (see PPC 405GP manual table 3-11 , page 3-14)
0xF000_0000	0xF000_001F	CAN-controller CAN 0
0xF000_0100	0xF000_011F	CAN-controller CAN 1
0xF020_0000	0xF020_7FFF	optional NVRAM
0xFFC0_0000	0xFFDF_FFFF	Flash-EPROM bank 0
0xFFE0_0000	0xFFFF_FFFF	Flash-EPROM bank 1

Table 3.1.1: Addresses

* The UARTs are 16550-compatible.

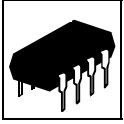


3.1.3 Interrupt-Assignment

Interrupt	External IRQ	Assignment	Level Detection
IRQ 25	EXT IRQ 0	CAN0	low active, level sensitive
IRQ26	EXT IRQ 1	CAN1	low active, level sensitive
IRQ 27	EXT IRQ 2	PCI-slot 0	low active, level sensitive
IRQ 28	EXT IRQ 3	PCI-slot 1	low active, level sensitive
IRQ 29	EXT IRQ 4	PCI-slot 2	low active, level sensitive
IRQ 30	EXT IRQ 5	PCI-slot 3	low active, level sensitive

Table 3.1.2: Assignment of the interrupts 25...30

All other interrupt sources are PPC 405GP -internal. They are described in the PowerPC 405GP manual.



Description of the Units

3.2 Serial Interface

3.2.1 Default Setting

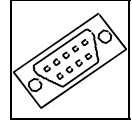
The default setting of the serial interfaces is:

Bit rate:	9600 Baud
Data bits:	8
Parity:	no
Stop bits:	1
Handshake:	XON/XOFF

3.2.2 Configuration

The serial interfaces are controlled by the PowerPC 405GP processor. The bit rates of the interfaces can be configured by the software. The serial controller integrated in the PPC 405GP and the RS-232-driver used for interface Serial 0 support bit rates of up to 115.2 kbit/s.

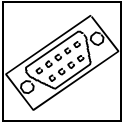
The procedure to change the bit rate depends on the operating system. Please refer to the manual of the operating system.



4. Connector Assignment

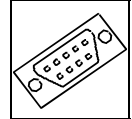
4.1 Assignment of the 64-pin PMC Connector P11 (Pn1/Jn1 32 Bit PCI)

Signal	Pin	Pin	Signal
n.c.	1	2	-12V
GND	3	4	INTA#
INTB#	5	6	INTC#
PRESENT#	7	8	VCC
INTD#	9	10	n.c.
GND	11	12	n.c.
PCI-CLK	13	14	GND
GND	15	16	GNT#
REQ#	17	18	VCC
V (I/O)	19	20	AD31
AD28	21	22	AD27
AD25	23	24	GND
GND	25	26	C/BE3#
AD22	27	28	AD21
AD19	29	30	GND
V (I/O)	31	32	AD17
FRAME#	33	34	GND
GND	35	36	IRDY#
DEVSEL#	37	38	VCC
GND	39	40	LOCK#
n.c.	41	42	n.c.
PAR	43	44	GND
V (I/O)	45	46	AD15
AD12	47	48	AD11
AD09	49	50	VCC
GND	51	52	C/BE0#
AD06	53	54	AD05
AD04	55	56	GND
V (I/O)	57	58	AD03
AD02	59	60	AD01
AD00	61	62	VCC
GND	63	64	n.c.



4.2 Assignment of the 64-pin PMC Connector P12 (PN2/Jn2 32 Bit PCI)

Signal	Pin	Pin	Signal
+12 V	1	2	n.c.
n.c.	3	4	TDO
TDI	5	6	GND
GND	7	8	n.c.
n.c.	9	10	n.c.
MODE2#	11	12	+3,3V
RST#	13	14	MODE3#
+3,3V	15	16	MODE4#
n.c.	17	18	GND
AD30	19	20	AD29
GND	21	22	AD26
AD24	23	24	+3,3V
IDSEL	25	26	AD23
+3,3V	27	28	AD20
AD18	29	30	GND
AD16	31	32	C/BE2#
GND	33	34	IDSELB
TRDY#	35	36	+3,3V
GND	37	38	STOP#
PERR#	39	40	GND
+3,3V	41	42	SERR#
C/BE1#	43	44	GND
AD14	45	46	AD13
GND	47	48	AD10
AD08	49	50	+3,3V
AD07	51	52	REQB#
+3,3V	53	54	GNTB#
n.c.	55	56	GND
n.c.	57	58	EREADEY
GND	59	60	RESETOUT#
n.c.	61	62	+3,3V
GND	63	64	MONARCH#

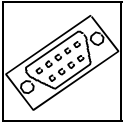


4.3 Assignment of the 64-pin PMC-I/O Connector P14 (CAN0, CAN1, Serial1)

The connector P14 (PN4/Jn4 32 bit PCI) has been assigned with the Rx/Tx-Signals of both CAN controllers and with the serial interface Serial 1. The CAN-signals are TTL-level and they are **not** electrically isolated from the microcontroller units.

Note: The pin assignment of connector P14 has changed from PCB reversion 1.0 to 1.1. The pin assignment of the connector shown in the table below is valid for boards from the serial number ABxxxx (delivery from October 2004).

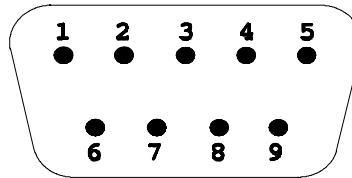
Signal	Pin	Pin	Signal
VCC	1	2	TX0-C0#
TX1-C0#	3	4	RX0-C0#
RX1-C0#	5	6	TX0-C1#
TX1-C1#	7	8	RX0-C1#
RX1-C1#	9	10	GND
GND	11	12	n.c.
n.c.	13	14	RXS1
n.c.	15	16	TXS1
CTSS1#	17	18	RTSS1#
n.c.	19	20	GND
n.c.	21	22	n.c.
	:	:	
	63	64	



Connector Assignment

4.4 Serial Interface Serial 0 at DSUB9 (X700)

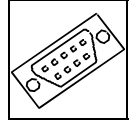
Pin Position:



Pin Assignment:

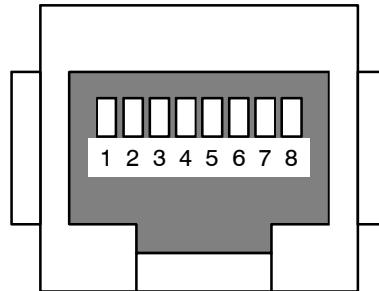
Signal	Pin		Signal
n.c.	6	1	n.c.
n.c.		2	RX
n.c.	7	3	TX
CTS		4	RTS
n.c.	9	5	GND

9-pin DSUB connector



4.5 ETHERNET 10/100BaseT Connector (X1100)

Pin Position:



Cut-out for
fastening lever

Pin Assignment:

Pin	Signal
1	TP01 (TxD+)
2	TP02 (TxD-)
3	TP03 (RxD+)
4	TP04
5	TP05
6	TP06 (RxD-)
7	TP07
8	TP08

8-pin RJ45-socket